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Nota di contenuto	1. Introductory concepts -- 1.1 Metallic interconnections -- 1.2 Simplified modeling of resistive interconnections as ladder networks -- 1.3 Propagation modes in a metallic interconnection -- 1.4 Slow-wave mode -- 1.5 Propagation delays -- 2. Modeling of interconnection resistances, capacitances, and inductances -- 2.1 Interconnection resistance -- 2.2 Modeling of resistance for a copper interconnection -- 2.3 Interconnection capacitances -- 2.4 The Green's function method, Method of images -- 2.5 Green's function method, Fourier integral approach -- 2.6 Interconnection inductances -- 2.7 Inductance extraction using FastHenry -- 2.8 Approximate equations for capacitances -- 2.9 Approximate equations for interconnection capacitances and inductances on silicon and GaAs substrates -- 3. Modeling of interconnection delays -- 3.1 Metal-insulator-semiconductor microstrip line model of an interconnection -- 3.2 Transmission line analysis of single-level interconnections -- 3.3 Transmission line model for multilevel interconnections -- 3.4 Modeling of parallel and crossing interconnections -- 3.5 Modeling of very-high-frequency losses in interconnections -- 3.6 Compact modeling of interconnection delays -- 3.7 Modeling of active interconnections -- 4. Modeling of interconnection crosstalk -- 4.1 Lumped capacitance

Sommario/riassunto

Quantitative understanding of the parasitic capacitances and inductances and the resultant propagation delays and crosstalk phenomena associated with the metallic interconnections on the very large scale integrated (VLSI) circuits has become extremely important for the optimum design of the state-of-the-art integrated circuits. It is because more than 65 percent of the delays on the integrated circuit chip occur in the interconnections and not in the transistors on the chip. Mathematical techniques to model the parasitic capacitances, inductances, propagation delays, crosstalk noise, and electromigration-induced failure associated with the interconnections in the realistic high-density environment on a chip will be discussed. An overview of the future interconnection technologies for the nanotechnology circuits will also be presented. This book will be the first book of its kind written for a one-semester course on the mathematical modeling of metallic interconnections on a VLSI circuit. In most institutions around the world offering BS, MS, and Ph.D. degrees in Electrical and Computer Engineering, such a course will be suitable for the first-year graduate students and it will also be appropriate as an elective course for senior level BS students. This book will also be of interest to practicing engineers in the field who are looking for a quick refresher on this subject.