

1. Record Nr.	UNINA9910459106603321
Titolo	Workforce intermediaries for the twenty-first century [[electronic resource] /] / edited by Robert P. Giloth
Pubbl/distr/stampa	Philadelphia, Pa., : Temple University Press, 2004
ISBN	1-282-65825-5 9786612658259 1-4399-0386-7
Descrizione fisica	1 online resource (433 p.)
Altri autori (Persone)	GilothRobert
Disciplina	331.25/92/0973
Soggetti	Hard-core unemployed - Services for - United States Welfare recipients - Employment - Government policy - United States Occupational training - Government policy - United States Employment agencies - United States Electronic books.
Lingua di pubblicazione	Inglese
Formato	Materiale a stampa
Livello bibliografico	Monografia
Note generali	"Published in association with the American Assembly, Columbia University."
Nota di bibliografia	Includes bibliographical references and index.
Nota di contenuto	Contents; Foreword / David H. Mortimer; I. Introduction; II. Who Are Workforce Intermediaries and What Do They Do?; III. Economic and Policy Rationales for Workforce Intermediaries; IV. Customer Voices; V. Building Workforce Intermediaries; VI. Conclusion; Appendix; About the Contributors; Acknowledgments; Index
Sommario/riassunto	Confronted with businesses facing a long-term shortage of skilled workers and evaluations showing that job training for the poor over the past 25 years had produced only meager results, a number of groups throughout the country have sought to find a more effective approach. The efforts of these partnerships, which editor Robert Giloth calls ""workforce intermediaries,"" are characterized by a focus on improving business productivity and helping low-income individuals not just find a job, but advance over time to jobs that enable them to support themselves and their families. This book takes st

2. Record Nr.	UNINA9910155575903321
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Titolo	Non-volatile in-memory computing by spintronics // Hao Yu, Leibin Ni, Yuhao Wang
Pubbl/distr/stampa	[San Rafael, California] : , : Morgan & Claypool Publishers, , 2017 ©2017
ISBN	1-62705-644-0
Descrizione fisica	1 online resource (163 pages) : color illustrations
Collana	Synthesis Lectures on Emerging Engineering Technologies, , 2381-1439
Disciplina	621.381
Soggetti	Spintronics Nonvolatile random-access memory
Lingua di pubblicazione	Inglese
Formato	Materiale a stampa
Livello bibliografico	Monografia
Note generali	Part of: Synthesis digital library of engineering and computer science.
Nota di bibliografia	Includes bibliographical references and index.
Nota di contenuto	1. Introduction -- 1.1 Memory wall -- 1.2 Traditional semiconductor memory -- 1.2.1 Overview -- 1.2.2 Nano-scale limitations -- 1.3 Non-volatile spintronic memory -- 1.3.1 Basic magnetization process -- 1.3.2 Magnetization damping -- 1.3.3 Spin-transfer torque -- 1.3.4 Magnetization dynamics -- 1.3.5 Domain wall propagation -- 1.4 Traditional memory architecture -- 1.5 Non-volatile in-memory computing architecture -- 1.6 References -- 2. Non-volatile spintronic device and circuit -- 2.1 SPICE formulation with new nano-scale NVM devices -- 2.1.1 Traditional modified nodal analysis -- 2.1.2 New MNA with non-volatile state variables -- 2.2 STT-MTJ device and model -- 2.2.1 STT-MTJ -- 2.2.2 STT-RAM -- 2.2.3 Topological insulator -- 2.3 Domain wall device and model -- 2.3.1 Magnetization reversal -- 2.3.2 MTJ resistance -- 2.3.3 Domain wall propagation -- 2.3.4 Circular domain wall nanowire -- 2.4 Spintronic storage -- 2.4.1 Spintronic memory -- 2.4.2 Spintronic readout -- 2.5 Spintronic logic -- 2.5.1 XOR -- 2.5.2 Adder -- 2.5.3 Multiplier -- 2.5.4 LUT -- 2.6 Spintronic interconnect -- 2.6.1 Coding-based interconnect -- 2.6.2 Domain wall-based encoder/decoder -- 2.6.3 Performance evaluation -- 2.7 References -- 3. In-memory data encryption -- 3.1 In-memory advanced encryption standard -- 3.1.1 Fundamental of AES -- 3.1.2 Domain wall nanowire-

based AES computing -- 3.1.3 Pipelined AES by domain wall nanowire -- 3.1.4 Performance evaluation -- 3.2 Domain wall-based SIMON block cipher -- 3.2.1 Fundamental of SIMON block cipher -- 3.2.2 Hardware stages -- 3.2.3 Round counter -- 3.2.4 Control signals -- 3.2.5 Key expansion -- 3.2.6 Encryption -- 3.2.7 Performance evaluation -- 3.3 References --
4. In-memory data analytics -- 4.1 In-memory machine learning -- 4.1.1 Extreme learning machine -- 4.1.2 MapReduce-based matrix multiplication -- 4.1.3 Domain wall-based hardware mapping -- 4.1.4 Performance evaluation -- 4.2 In-memory face recognition -- 4.2.1 Energy-efficient STT-MRAM with Spare-represented data -- 4.2.2 QoS-aware adaptive current scaling -- 4.2.3 STT-RAM based hardware mapping -- 4.2.4 Performance evaluation -- 4.3 References --
Authors' biographies.

Sommario/riassunto

Exa-scale computing needs to re-examine the existing hardware platform that can support intensive data-oriented computing. Since the main bottleneck is from memory, we aim to develop an energy-efficient in-memory computing platform in this book. First, the models of spin-transfer torque magnetic tunnel junction and racetrack memory are presented. Next, we show that the spintronics could be a candidate for future data-oriented computing for storage, logic, and interconnect. As a result, by utilizing spintronics, in-memory-based computing has been applied for data encryption and machine learning. The implementations of in-memory AES, Simon cipher, as well as interconnect are explained in details. In addition, in-memory-based machine learning and face recognition are also illustrated in this book.
