1. Record Nr. UNINA9910458595103321

Autore	Benini Luca <1967->
Titolo	Networks on chips [[electronic resource]] : technology and tools / / Luca Benini and Giovanni De Micheli
Pubbl/distr/stampa	Amsterdam ; ; Boston, : Elsevier Morgan Kaufmann Publishers, c2006
ISBN	1-280-96683-1 9786610966837 0-08-047356-3
Edizione	[1st edition]
Descrizione fisica	1 online resource (408 p.)
Collana	The Morgan Kaufmann series in systems on silicon
Altri autori (Persone)	De MicheliGiovanni
Disciplina	621.3815
Soggetti	Systems on a chip Computer networks - Equipment and supplies Electronic books.
Lingua di pubblicazione	Inglese
Formato	Materiale a stampa
Livello bibliografico	Monografia
Note generali	Description based upon print version of record.
Nota di bibliografia	Includes bibliographical references and index.
Nota di contenuto	Front Cover; Title page; Copyright Page; Table of contents; About The Authors; List of Contributors; 1 Networks on Chip; 1.1 Why On-Chip Networking?; 1.2 Technology Trends; 1.3 SoC Objectives and NoC Needs; 1.4 Once Over Lightly; 1.5 Perspectives; 2 Network Architecture: Principles and Examples; 2.1 Network Architecture; 2.2 Network Architectures for On-Chip Realization; 2.3 Ad Hoc Network Architectures; 2.4 Component Design for NoCs; 2.5 Properties of Network Architectures; 2.6 Summary; 3 Physical Network Layer; 3.1 Interconnection in DSM SoC; 3.2 High-Performance Signaling 3.3 Building Blocks3.4 Summary; 4 The Data-Link Layer in NoC Design; 4.1 Tasks of the Data-Link Layer; 4.2 On-Chip Communication Reliability; 4.3 Fault Models for NoCs; 4.4 Principles of Coding Theory; 4.5 The Power-Reliability Trade-Off; 4.6 Unified Coding Framework; 4.7 Adaptive Error Protection; 4.8 Data-Link Layer Architecture: Case Studies; 4.9 On-Chip Stochastic Communication; 4.10 Link-Level versus End-to-End Error Protection; 4.11 Flow Control; 4.12 Performance Exploration; 4.13 Summary; 5 Network and Transport Layers in Network on Chip; 5.1 Network and Transport Layers in NoCs 5.2 NoC QoS5.3 NoC Topology; 5.4 Switching Techniques; 5.5 NoC

Addressing and Routing; 5.6 NoC Addressing; 5.7 Congestion Control and Flow Control; 5.8 Summary; 6 Network Interface Architecture and Design Issues; 6.1 NI Services; 6.2 NI Structure; 6.3 Evolution of Communication Protocols; 6.4 Point-to-Point Communication Protocols; 6.5 Latest Advances in Processor Interfaces; 6.6 The Packetization Stage; 6.7 End-to-End Flow Control; 6.8 Packet and Circuit Switching; 6.9 NI Architecture: The Aethereal Case Study; 6.10 NI Architecture: The xpipes Case Study
6.11 NIs for Asynchronous NoCs: The Mango Case Study6.12 Summary; 7 NoC Programming; 7.1 Architectural Template; 7.2 Task-Level Parallel Programming; 7.3 Communication-Exposed Programming; 7.4 Computer-Aided Software Development Tools; 7.5 Summary; 8 Design Methodologies and CAD Tool Flows for NoCs; 8.1 Network Analysis and Simulation; 8.2 Network Synthesis and Optimization; 8.3 Design Flows for NoCs; 8.4 Tool Kits for Designing Bus-Based Interconnect; 8.5 Summary; 9 Designs and Implementations of NoC-Based SoCs; 9.1 KAIST BONE Series; 9.2 NoC-Based Experimental Systems; 9.3 Summary; Index

Sommario/riassunto

The design of today's semiconductor chips for various applications, such as telecommunications, poses various challenges due to the complexity of these systems. These highly complex systems-on-chips demand new approaches to connect and manage the communication between on-chip processing and storage components and networks on chips (NoCs) provide a powerful solution. This book is the first to provide a unified overview of NoC technology. It includes in-depth analysis of all the on-chip communication challenges, from physical wiring implementation up to software architecture, and a compl