

1. Record Nr.	UNINA9910457721703321
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Titolo	Low-voltage CMOS RF frequency synthesizers / / Howard Cam Luong and Gerry Chi Tak Leung [[electronic resource]]
Pubbl/distr/stampa	Cambridge : , : Cambridge University Press, , 2004
ISBN	1-107-15045-0 1-280-54060-5 9786610540600 0-511-21493-6 0-511-21672-6 0-511-21135-X 0-511-31546-5 0-511-54114-7 0-511-21312-3
Descrizione fisica	1 online resource (xvii, 180 pages) : digital, PDF file(s)
Disciplina	621.3815/486
Soggetti	Frequency synthesizers - Design and construction Metal oxide semiconductors, Complementary - Design and construction
Lingua di pubblicazione	Inglese
Formato	Materiale a stampa
Livello bibliografico	Monografia
Note generali	Title from publisher's bibliographic system (viewed on 05 Oct 2015).
Nota di bibliografia	Includes bibliographical references (p. 173-177) and index.
Nota di contenuto	; 1. Introduction -- ; 2. Synthesizer fundamentals -- ; 3. Design of building blocks -- ; 4. Low-voltage design considerations and techniques -- ; 5. Behavioral simulation -- ; 6. A 2 V 900 MHz monolithic CMOS dual-loop frequency synthesizer for GSM receivers -- ; 7. A 1.5 V 900 MHz monolithic CMOS fast-switching frequency synthesizer for wireless applications -- ; 8. A 1 V 5.2 GHz fully integrated CMOS synthesizer for WLAN IEEE 802.11a.
Sommario/riassunto	A frequency synthesizer is one of the most critical building blocks in any wireless transceiver system. Its design is getting more and more challenging as the demand for low-voltage low-power high-frequency wireless systems continuously grows. As the supply voltage is decreased, many existing design techniques are no longer applicable. This book provides the reader with architectures and design techniques

to enable CMOS frequency synthesizers to operate at low supply voltage at high frequency with good phase noise and low power consumption. In addition to updating the reader on many of these techniques in depth, this book will also introduce useful guidelines and step-by-step procedure on behaviour simulations of frequency synthesizers. Finally, three successfully demonstrated CMOS synthesizer prototypes with detailed design consideration and description will be elaborated to illustrate potential applications of the architectures and design techniques described. For engineers, managers and researchers working in radio-frequency integrated-circuit design for wireless applications.
