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Nota di contenuto	Front Cover; The Definitive Guide to the ARM Cortex-M3; Copyright Page; Table of Contents; Foreword; Preface; Acknowledgments; Terms and Abbreviations; Conventions; References; Chapter 1 - Introduction; What Is the ARM Cortex-M3 Processor?; Background of ARM and ARM Architecture; A Brief History; Architecture Versions; Processor Naming; Instruction Set Development; The Thumb-2 Instruction Set Architecture (ISA); Cortex-M3 Processor Applications; Organization of This Book; Further Readings; Chapter 2 - Overview of the Cortex-M3; Fundamentals; Registers; R0 to R12: General-Purpose Registers R13: Stack PointersR14: The Link Register; R15: The Program Counter; Special Registers; Operation Modes; The Built-In Nested Vectored Interrupt Controller; Nested Interrupt Support; Vectored Interrupt Support; Dynamic Priority Changes Support; Reduction of Interrupt Latency; Interrupt Masking; The Memory Map; The Bus Interface; The Memory Protection Unit; The Instruction Set; Interrupts and Exceptions; Debugging Support; Characteristics Summary; High Performance; Advanced Interrupt-Handling Features; Low Power Consumption; System Features; Debug Supports; Chapter 3 - Cortex-M3 Basics

RegistersGeneral-Purpose Registers R0-R7; General-Purpose Registers R8-R12; Stack Pointer R13; Link Register R14; Program Counter R15; Special Registers; Program Status Registers (PSRs); PRIMASK, FAULTMASK, and BASEPRI Registers; The Control Register; Operation Mode; Exceptions and Interrupts; Vector Tables; Stack Memory Operations; Basic Operations of the Stack; Cortex-M3 Stack Implementation; The Two-Stack Model in the Cortex-M3; Reset Sequence; Chapter 4 - Instruction Sets; Assembly Basics; Assembler Language: Basic Syntax; Assembler Language: Use of Suffixes Assembler Language: Unified Assembler LanguageInstruction List; Unsupported Instructions; Instruction Descriptions; Assembler Language: Moving Data; LDR and ADR Pseudo Instructions; Assembler Language: Processing Data; Assembler Language: Call and Unconditional Branch; Assembler Language: Decisions and Conditional Branches; Assembler Language: Combined Compare and Conditional Branch; Assembler Language: Conditional Branches Using IT Instructions; Assembler Language: Instruction Barrier and Memory Barrier Instructions; Assembly Language: Saturation Operations Several Useful Instructions in the Cortex-M3MSR and MRS; IF-THEN; CBZ and CBNZ; SDIV and UDIV; REV, REVH, and REVSH; RBIT; SXTB, SXTH, UXTB, and UXTH; BFC and BFI; UBFX and SBFX; LDRD and STRD; TBB and TBH; Chapter 5 - Memory Systems; Memory System Features Overview; Memory Maps; Memory Access Attributes; Default Memory Access Permissions; Bit-Band Operations; Advantages of Bit-Band Operations; Bit-Band Operation of Different Data Sizes; Bit-Band Operations in C Programs; Unaligned Transfers; Exclusive Accesses; Endian Mode; Chapter 6 - Cortex-M3 Implementation Overview; The Pipeline
A Detailed Block Diagram

Sommario/riassunto

This user's guide does far more than simply outline the ARM Cortex-M3 CPU features; it explains step-by-step how to program and implement the processor in real-world designs. It teaches readers how to utilize the complete and thumb instruction sets in order to obtain the best functionality, efficiency, and reuseability. The author, an ARM engineer who helped develop the core, provides many examples and diagrams that aid understanding. Quick reference appendices make locating specific details a snap! Whole chapters are dedicated to: Debugging using the new CoreSight technologyMi