1. Record Nr. UNINA9910455172203321

Autore	Quemada Carlos
Titolo	Design methodology for RF CMOS phase locked loops / / Carlos Quemada, Guillermo Bistue, Ianigo Adin
Pubbl/distr/stampa	Boston : , : Artech House, , ©2009 [Piscataqay, New Jersey] : , : IEEE Xplore, , [2008]
ISBN	1-59693-384-4
Descrizione fisica	1 online resource (242 p.)
Collana	Artech House microwave library
Altri autori (Persone)	BistueGuillermo AdinIanigo
Disciplina	621.3815/364
Soggetti	Metal oxide semiconductors, Complementary - Design and construction Phase-locked loops - Design and construction Electronic books.
Lingua di pubblicazione	Inglese
Formato	Materiale a stampa
Livello bibliografico	Monografia
Note generali	Description based upon print version of record.
Nota di bibliografia	Includes bibliographical references and index.
Nota di contenuto	Design Methodology for RF CMOS Phase Locked Loops; Contents; Preface; 1 Approach to CMOS PLL Design; 2 PLL Fundamentals; 3 LC-Tank Integrated Oscillators; 4 Frequency Divider; 5 Phase Frequency Detector/Phase Detector; 6 Determination of Building Blocks Specifications; 7 Design of a 3.2-GHz CMOS VCO; 8 Design of a Frequency Divider; 9 Design of a Phase Frequency Detector; 10 Design of the Complete PLL; 11 PLL Characterization and Results; About the Authors; Index
Sommario/riassunto	Blast through phase-locked loop challenges fast with this practical book guiding you every step of the way from specs definition to layout generation. You get a proven PLL design and optimization methodology that lets you systematically assess design alternatives, predict PLL behavior, and develop complete PLLs for CMOS applications that meet performance requirements no matter what IC challenges you come up against. After a review of PLL essentials, this uniquely comprehensive workbench guide takes you step-by-step through operation principles, design procedures, phase noise analysis, layout considerations, and CMOS realizations for each PLL building block. You get full details on

LC tank oscillators including modeling and optimization techniques, followed by design options for CMOS frequency dividers covering flip-flop implementation, the divider by 2 component, and other key factors. The book includes design alternatives for phase detectors that feature methods to minimize jitter caused by the dead zone effect. You also find a sample design of a fully integrated PLL for WLAN applications that demonstrates every step and detail right down to the circuit schematics and layout diagrams. Supported by over 150 diagrams and photos, this one-stop toolkit helps you produce superior PLL designs faster, and deliver more effective solutions for low-cost integrated circuits in all RF applications.