1. Record Nr. UNINA9910454996503321

Titolo	Clinical approach to infection in the compromised host [[electronic resource] /] / edited by Robert H. Rubin and Lowell S. Young ; with a foreword by Ralph Van Furth
Pubbl/distr/stampa	New York, : Kluwer Academic/Plenum, c2002
ISBN	1-280-20014-6 9786610200146 0-306-47527-8
Edizione	[4th ed.]
Descrizione fisica	1 online resource (760 p.)
Altri autori (Persone)	RubinRobert H. <1941-> YoungLowell S
Disciplina	616.9/0479
Soggetti	Opportunistic infections Communicable diseases Immunological deficiency syndromes - Complications Electronic books.
Lingua di pubblicazione	Inglese
Formato	Materiale a stampa
Livello bibliografico	Monografia
Note generali	Description based upon print version of record.
Nota di bibliografia	Includes bibliographical references and index.
Nota di contenuto	Defects in Host Defense Mechanisms -- Mucocutaneous Infections in the Immunocompromised Host -- Clinical Approach to the Compromised Host with Fever and Pulmonary Infiltrates -- Central Nervous System Infection in the Immunocompromised Host -- Fungal Infections in the Immunocompromised Host -- Mycobacterial and Nocardial Diseases in the Compromised Host -- Pneumocystis carinii and Parasitic Infections in the Immunocompromised Host -- Viral Hepatitis in the Compromised Host -- The Herpesviruses -- Morbidity in Compromised Patients Related to Viruses Other than Herpes Group and Hepatitis Viruses -- Pathogenesis and Clinical Manifestations of HIV-1 Infection -- Infectious Complications in Children with Cancer and Children with Human Immunodeficiency Virus Infection -- Infections Complicating Congenital Immunodeficiency Syndromes -- Management of Infections in Leukemia and Lymphoma -- Infection in Hematopoietic Stem Cell Transplantation -- Infection in the Organ Transplant Recipient -- Surgical Aspects of Infection in the

	Compromised Host.
Sommario/riassunto	At the beginning of the new millennium, it is opportune to review what has been accomplished in the field of infectious diseases during the last decades of the previous century. The paradigm of the immunocompromised host gene has taught much about the pathophysiology of infectious diseases, particularly with regard to immunological aspects of host defense. In the beginning, Robert Good called immunodeficiency syndromes “experiments of nature. ” In the 1960's and subsequent decades, the clinical and immunological aspects of immune deficiencies were studied and adequate treatment attempted. A reflection of these developments were the three successful meetings on these topics in Veldhoven, The Netherlands (1980), Stirling, Scotland. Since then, the IIHS has organized meetings every two years...

2.

Record Nr.	UNISA996465962903316
Titolo	Integrated Circuit and System Design. Power and Timing Modeling, Optimization and Simulation [[electronic resource]] : 18th International Workshop, PATMOS 2008, Lisbon, Portugal, September 10-12, 2008, Revised Selected Papers / / edited by Lars Svensson, José Monteiro
Pubbl/distr/stampa	Berlin, Heidelberg : , : Springer Berlin Heidelberg : , : Imprint : Springer, , 2009
ISBN	3-540-95948-3
Edizione	[1st ed. 2009.]
Descrizione fisica	1 online resource (XIII, 462 p.)
Collana	Theoretical Computer Science and General Issues, , 2512-2029 ; ; 5349
Classificazione	DAT 190f ELT 272f SS 4800
Disciplina	620/.004202825536
Soggetti	Logic design Microprocessors Computer architecture Electronic digital computers—Evaluation Computer arithmetic and logic units Computer storage devices Memory management (Computer science) Electronic circuits Logic Design Processor Architectures System Performance and Evaluation Arithmetic and Logic Structures

	Computer Memory Structure Electronic Circuits and Systems
Lingua di pubblicazione	Inglese
Formato	Materiale a stampa
Livello bibliografico	Monografia
Note generali	Bibliographic Level Mode of Issuance: Monograph
Nota di bibliografia	Includes bibliographical references and index.
Nota di contenuto	Session 1: Low-Leakage and Subthreshold Circuits -- Subthreshold FIR Filter Architecture for Ultra Low Power Applications -- Reverse Vgs Static CMOS (RVGS-SCMOS); A New Technique for Dynamically Compensating the Process Variations in Sub-threshold Designs -- Improving the Power-Delay Performance in Subthreshold Source-Coupled Logic Circuits -- Design and Evaluation of Mixed 3T-4T FinFET Stacks for Leakage Reduction -- Session 2: Low-Power Methods and Models -- Temporal Discharge Current Driven Clustering for Improved Leakage Power Reduction in Row-Based Power-Gating -- Intelligate: Scalable Dynamic Invariant Learning for Power Reduction -- Analysis of Effects of Input Arrival Time Variations on On-Chip Bus Power Consumption -- Power-Aware Design via Micro-architectural Link to Implementation -- Untraditional Approach to Computer Energy Reduction -- Session 3: Arithmetic and Memories -- Mixed Radix-2 and High-Radix RNS Bases for Low-Power Multiplication -- Power Optimization of Parallel Multipliers in Systems with Variable Word-Length -- A Design Space Comparison of 6T and 8T SRAM Core-Cells -- Latched CMOS DRAM Sense Amplifier Yield Analysis and Optimization -- Session 4: Variability and Statistical Timing -- Understanding the Effect of Intradie Random Process Variations in Nanometer Domino Logic -- A Study on CMOS Time Uncertainty with Technology Scaling -- Static Timing Model Extraction for Combinational Circuits -- A New Bounding Technique for Handling Arbitrary Correlations in Path-Based SSTA -- Statistical Modeling and Analysis of Static Leakage and Dynamic Switching Power -- Session 5: Synchronization and Interconnect -- Logic Synthesis of Handshake Components Using Structural Clustering Techniques -- Fast Universal Synchronizers -- A Performance-Driven Multilevel Framework for the X-Based Full-Chip Router -- PMD: A Low-Power Code for Networks-on-Chip Based on Virtual Channels -- Session 6: Power Supplies and Switching Noise -- Near-Field Mapping System to Scan in Time Domain the Magnetic Emissions of Integrated Circuits -- A Comparison between Two Logic Synthesis Forms from Digital Switching Noise Viewpoint -- Generating Worst-Case Stimuli for Accurate Power Grid Analysis -- Monolithic Multi-mode DC-DC Converter with Gate Voltage Optimization -- Session 7: Low-Power Circuits; Reconfigurable Architectures -- Energy Efficiency of Power-Gating in Low-Power Clocked Storage Elements -- A New Dynamic Logic Circuit Design for an Effective Trade-Off between Noise-Immunity, Performance and Energy Dissipation -- Energy Efficient Elliptic Curve Processor -- Energy Efficient Coarse-Grain Reconfigurable Array for Accelerating Digital Signal Processing -- Power-Efficient Reconfiguration Control in Coarse-Grained Dynamically Reconfigurable Architectures -- Poster Session 1: Circuits and Methods -- Settling-Optimization-Based Design Approach for Three-Stage Nested-Miller Amplifiers -- Ultra Low Voltage High Speed Differential CMOS Inverter -- Differential

Capacitance Analysis -- Automated Synchronous-to-Asynchronous Circuits Conversion: A Survey -- Novel Cross-Transition Elimination Technique Improving Delay and Power Consumption for On-Chip Buses -- Poster Session 2: Power and Delay Modeling -- Analytical High-Level Power Model for LUT-Based Components -- A Formal Approach for Estimating Embedded System Execution Time and Energy Consumption -- Power Dissipation Associated to Internal Effect Transitions in Static CMOS Gates -- Disjoint Region Partitioning for Probabilistic Switching Activity Estimation at Register Transfer Level -- Data Dependence of Delay Distribution for a Planar Bus -- Special Session: Power Optimizations Addressing Reconfigurable Architectures -- Towards Novel Approaches in Design Automation for FPGA Power Optimization -- Smart Enumeration: A Systematic Approach to Exhaustive Search -- An Efficient Approach for Managing Power Consumption Hotspots Distribution on 3D FPGAs -- Interconnect Power Analysis for a Coarse-Grained Reconfigurable Array Processor -- Keynotes (Abstracts) -- Integration of Power Management Units onto the SoC -- Model to Hardware Matching for nm Scale Technologies -- Power and Profit: Engineering in the Envelope.

Sommario/riassunto

This book constitutes the thoroughly refereed post-conference proceedings of 18th International Workshop on Power and Timing Modeling, Optimization and Simulation, PATMOS 2008, featuring Integrated Circuit and System Design, held in Lisbon, Portugal during September 10-12, 2008. The 31 revised full papers and 10 revised poster papers presented together with 3 invited talks and 4 papers from a special session on reconfigurable architectures were carefully reviewed and selected from numerous submissions. The papers are organized in topical sections on low-leakage and subthreshold circuits, low-power methods and models, arithmetic and memories, variability and statistical timing, synchronization and interconnect, power supplies and switching noise, low-power circuits; reconfigurable architectures, circuits and methods, power and delay modeling, as well as power optimizations addressing reconfigurable architectures.