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Nota di contenuto	Model checking and equivalence checking / Masahiro Fujita -- Transaction-level system modeling / Daniel Gajski and Samar Abdi -- Response checkers, monitors, and assertions / Harry Foster -- System debugging strategies / Wayne H. Wolf -- Test generation and coverage metrics / Ernesto Sanchez, Giovanni Squillero, and Matteo Sonza Reorda -- SystemVerilog and Vera in a verification flow / Shireesh Verma and Ian G. Harris -- Decision diagrams for verification / Maciej Ciesielski, Dhiraj K. Pradhan, and Abusaleh M. Jabir -- Boolean satisfiability and EDA applications / Joao Marques-Silva.
Sommario/riassunto	Improve design efficiency and reduce costs with this practical guide to formal and simulation-based functional verification. Giving you a theoretical and practical understanding of the key issues involved, expert authors including Wayne Wolf and Dan Gajski explain both formal techniques (model checking, equivalence checking) and

simulation-based techniques (coverage metrics, test generation). You get insights into practical issues including hardware verification languages (HVLs) and system-level debugging. The foundations of formal and simulation-based techniques are covered too, as are more recent research advances including transaction-level modeling and assertion-based verification, plus the theoretical underpinnings of verification, including the use of decision diagrams and Boolean satisfiability (SAT).