1. Record Nr. UNINA9910452273903321

Autore	Peterson Sarah E. <1983->
Titolo	Thin-section petrography of ceramic materials [[electronic resource] /] / by Sarah E. Peterson ; with contributions by Philip P. Betancourt
Pubbl/distr/stampa	Philadelphia, Pa., : INSTAP Academic Press, c2009
ISBN	1-62303-126-5
Descrizione fisica	1 online resource (33 p.)
Collana	INSTAP archaeological excavation manual ; ; v. 2
Altri autori (Persone)	BetancourtPhilip P. <1936->
Disciplina	552/.06
Soggetti	Petrology in archaeology Ceramics - Analysis Electronic books.
Lingua di pubblicazione	Inglese
Formato	Materiale a stampa
Livello bibliografico	Monografia
Note generali	Description based upon print version of record.
Nota di bibliografia	Includes bibliographical references (p. [17]-20).
Nota di contenuto	Goals for the thin-section petrography of ceramics -- History of thin-section petrography -- Preparation of thin sections -- Examination and analysis of thin sections -- Development of aims and sampling strategy.
Sommario/riassunto	As part of the INSTAP Archaeological Excavation Manual series, Thin-Section Petrography of Ceramic Materials provides a concise overview of the history and application of the practice while detailing how this type of petrographic analysis can benefit archaeologists in the field. When thin-section analysis is employed as part of a thorough, multi-disciplinary study of ceramic materials, it provides a wealth of additional interpretative data to archaeologists, allowing for more accurate interpretations of the past, especially regarding pottery production, provenance, variations in technology ove

2. Record Nr. UNINA9910409666503321

Autore	Lutsyk Petro
Titolo	A Pipelined Multi-Core Machine with Operating System Support : Hardware Implementation and Correctness Proof / / by Petro Lutsyk, Jonas Oberhauser, Wolfgang J. Paul
Pubbl/distr/stampa	Cham : , : Springer International Publishing : , : Imprint : Springer, , 2020
ISBN	3-030-43243-2
Edizione	[1st ed. 2020.]
Descrizione fisica	1 online resource (634 pages)
Collana	Theoretical Computer Science and General Issues, , 2512-2029 ; ; 9999
Disciplina	005.434
Soggetti	Computer programming Computer engineering Computer networks Microprogramming Computer input-output equipment Logic programming Computer science Programming Techniques Computer Engineering and Networks Control Structures and Microprogramming Input/Output and Data Communications Logic in AI Theory of Computation
Lingua di pubblicazione	Inglese
Formato	Materiale a stampa
Livello bibliografico	Monografia
Nota di contenuto	Introductory material -- on hierarchical hardware design -- hardware library -- basic processor design -- pipelining -- cache memory systems -- interrupt mechanism -- self modification, instruction buffer and nondeterministic ISA -- memory management units -- store buffers -- multi-core processors -- advanced programmable interrupt controllers (APICs) -- adding a disk -- I/O apic.
Sommario/riassunto	This work is building on results from the book named “A Pipelined Multi-core MIPS Machine: Hardware Implementation and Correctness”

by M. Kovalev, S.M. Müller, and W.J. Paul, published as LNCS 9000 in 2014. It presents, at the gate level, construction and correctness proof of a multi-core machine with pipelined processors and extensive operating system support with the following features: • MIPS instruction set architecture (ISA) for application and for system programming • cache coherent memory system • store buffers in front of the data caches • interrupts and exceptions • memory management units (MMUs) • pipelined processors: the classical five-stage pipeline is extended by two pipeline stages for address translation • local interrupt controller (ICs) supporting inter-processor interrupts (IPIs) • I/O-interrupt controller and a disk .