1. Record Nr. UNINA9910451878903321

Titolo	Communicating process architectures 2007 [[electronic resource]] : WoTUG-30 : proceedings of the 30th WoTUG Technical Meeting, 8-11 July 2007, University of Surrey, Guildford, United Kingdom / / edited by Alistair A. McEwan ... [et al.]
Pubbl/distr/stampa	Amsterdam ; Fairfax, VA, : IOS Press, 2007
ISBN	6611029842 1-281-02984-X 9786611029845 1-60750-261-5 600-00-0368-4 1-4356-0867-4
Descrizione fisica	1 online resource (528 p.)
Collana	Concurrent systems engineering series ; ; v. 65
Altri autori (Persone)	McEwanAlistair A
Disciplina	004
Soggetti	Parallel processing (Electronic computers) occam (Computer program language) Transputers Computer architecture Electronic books.
Lingua di pubblicazione	Inglese
Formato	Materiale a stampa
Livello bibliografico	Monografia
Note generali	Description based upon print version of record.
Nota di contenuto	Title page; Preface; Programme Committee; Additional Reviewers; Contents; Fine-Grain Concurrency; Communicating Process Architecture for Multicores; Lazy Exploration and Checking of CSP Models with CSPsim; The Core Language of Aldwych; JCSProB: Implementing Integrated Formal Specifications in Concurrent Java; Components with Symbolic Transition Systems: A Java Implementation of Rendezvous; Concurrent/Reactive System Design with Honeysuckle; CSP and Real-Time: Reality or Illusion?; Testing and Sampling Parallel Systems; Mobility in JCSP: New Mobile Channel and Mobile Process Models C++CSP2: A Many-to-Many Threading Model for Multicore ArchitecturesDesign Principles of the SystemCSP Software Framework;

PyCSP - Communicating Sequential Processes for Python; A Process-Oriented Architecture for Complex System Modelling; Concurrency Control and Recovery Management for Open e-Business Transactions; trancell - An Experimental ETC to Cell BE Translator; A Versatile Hardware-Software Platform for In-Situ Monitoring Systems; High Cohesion and Low Coupling: The Office Mapping Factor; A Process Oriented Approach to USB Driver Development
A Native Transterpreter for the LEGO Mindstorms RCXIntegrating and Extending JCSP; Hardware/Software Synthesis and Verification Using Esterel; Modeling and Analysis of the AMBA Bus Using CSP and B; A Step Towards Refining and Translating B Control Annotations to Handel-C; Towards the Formal Verification of a Java Processor in Event-B; Advanced System Simulation, Emulation and Test (ASSET); Development of a Family of Multi-Core Devices Using Hierarchical Abstraction; Domain Specific Transformations for Hardware Ray Tracing
A Reconfigurable System-on-Chip Architecture for Pico-Satellite MissionsTransactional CSP Processes; Algebras of Actions in Concurrent Processes; Using occam-pi Primitives with the Cell Broadband Engine; Shared-Memory Multi-Processor Scheduling Algorithms for CCSP; Compiling occam to C with Tock; Author Index

Sommario/riassunto

Deals with Computer Science and models of Concurrency. This title emphasizes on hardware/software co-design and the understanding of concurrency that results from these systems. It includes a range of papers on this topic, from the formal modeling of buses in co-design systems through to software simulation and development environments.