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Nota di contenuto	Front Cover; VHDL-2008: Just the New Stuff; Copyright Page; Contents; Preface; Chapter 1. Enhanced Generics; 1.1 Generic Types; 1.2 Generic Lists in Packages; 1.3 Local Packages; 1.4 Generic Lists in Subprograms; 1.5 Generic Subprograms; 1.6 Generic Packages; 1.7 Use Case: Generic Memories; Chapter 2. Other Major Features; 2.1 External Names; 2.2 Force and Release; 2.3 Context Declarations; 2.4 Integrated PSL; 2.5 IP Encryption; 2.6 VHDL Procedural Interface (VHPI); Chapter 3. Type System Changes; 3.1 Unconstrained Element Types; 3.2 Resolved Elements; Chapter 4. New and Changed Operations 4.1 Array/Scalar Logical Operations 4.2 Array/Scalar Addition Operators; 4.3 Logical Reduction Operators; 4.4 Condition Operator; 4.5 Matching Relational Operators; 4.6 Maximum and Minimum; 4.7 Mod and Rem for Physical Types; 4.8 Shift Operations; 4.9 Strength Reduction and 'X' Detection; Chapter 5. New and Changed Statements; 5.1 Conditional and Selected Assignments; 5.2 Matching Case Statements; 5.3 If and Case Generate; Chapter 6. Modeling Enhancements; 6.1 Signal Expressions in Port Maps; 6.2 All Signals in Sensitivity List; 6.3 Reading Out-Mode Ports and Parameters 6.4 Slices in Aggregates 6.5 Bit-String Literals; Chapter 7. Improved I/O; 7.1 The To_string Functions; 7.2 The Justify Function; 7.3 Newline Formatting; 7.4 Read and Write Operations; 7.5 The Tee Procedure; 7.6

	The Flush Procedure; Chapter 8. Standard Packages; 8.1 The Std_logic_1164 Package; 8.2 The Numeric_bit and Numeric_std Packages; 8.3 The Numeric Unsigned Packages; 8.4 The Fixed-Point Math Packages; 8.5 The Floating-Point Math Packages; 8.6 The Standard Package; 8.7 The Env Package; 8.8 Operator Overloading Summary; 8.9 Conversion Function Summary 8.10 Strength Reduction Function Summary Chapter 9. Miscellaneous Changes; 9.1 Referencing Generics in Generic Lists; 9.2 Function Return Subtype; 9.3 Qualified Expression Subtype; 9.4 Type Conversions; 9.5 Case Expression Subtype; 9.6 Subtypes for Port and Parameter Actuals; 9.7 Static Composite Expressions; 9.8 Static Ranges; 9.9 Use Clauses, Types, and Operations; 9.10 Hiding of Implicit Operations; 9.11 Multidimensional Array Alias; 9.12 Others in Aggregates; 9.13 Attribute Specifications in Package Bodies; 9.14 Attribute Specification for Overloaded Subprograms 9.15 Integer Expressions in Range Bounds 9.16 Action on Assertion Violations; 9.17 'Path_Name and 'Instance_Name; 9.18 Non-Nesting of Architecture Region; 9.19 Purity of Now; 9.20 Delimited Comments; 9.21 Tool Directives; 9.22 New Reserved Words; 9.23 Replacement Characters; Chapter 10. What's Next; 10.1 Object-Oriented Class Types; 10.2 Randomization; 10.3 Functional Coverage; 10.4 Alternatives; 10.5 Getting Involved; Index
Sommario/riassunto	VHDL-2008: Just the New Stuff, as its title says, introduces the new features added to the latest revision of the IEEE standard for the VHDL hardware description language. Written by the Chair and Technical Editor of the IEEE working group, the book is an authoritative guide to how the new features work and how to use them to improve design productivity. It will be invaluable for early adopters of the new language version, for tool implementers, and for those just curious about where VHDL is headed.* First in the market describing the new features of VHDL 2008;* Just the new featur