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Nota di bibliografia	Includes bibliographical references and index.
Nota di contenuto	Introduction -- Probabilistic Transfer Matrices -- Computing with Probabilistic Transfer Matrices -- Testing Logic Circuits for Probabilistic Faults -- Signtaure-based Reliability Analysis -- Design for Robustness -- Summary and Extensions.
Sommario/riassunto	Integrated circuits (ICs) increasingly exhibit uncertain characteristics due to soft errors, inherently probabilistic devices, and manufacturing variability. As device technologies scale, these effects can be detrimental to the reliability of logic circuits. To improve future semiconductor designs, this book describes methods for analyzing, designing, and testing circuits subject to probabilistic effects. The authors first develop techniques to model inherently probabilistic methods in logic circuits and to test circuits for determining their reliability after they are manufactured. Then, they study error-masking mechanisms intrinsic to digital circuits and show how to leverage them to design more reliable circuits. The book describes techniques for: • Modeling and reasoning about probabilistic behavior in logic circuits, including a matrix-based reliability-analysis framework; • Accurate analysis of soft-error rate (SER) based on functional-simulation, sufficiently scalable for use in gate-level optimizations; • Logic synthesis for greater resilience against soft

errors, which improves reliability using moderate overhead in area and performance; • Test-generation and test-compaction methods aimed at probabilistic faults in logic circuits that facilitate accurate and efficient post-manufacture measurement of soft-error susceptibility.