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Nota di bibliografia	Includes bibliographical references.
Nota di contenuto	Part I: Introduction and Prior Art -- Timing Closure for Multi-Million-Gate Integrated Circuits -- State of the Art in Physical Synthesis -- Part II: Local Physical Synthesis and Necessary Analysis Techniques -- Buffer Insertion during Timing-Driven Placement -- Bounded Transactional Timing Analysis -- Gate Sizing During Timing-Driven Placement -- Part III: Broadening the Scope of Circuit Transformations -- Physically-Driven Logic Restructuring -- Logic Restructuring as an Aid to Physical Retiming -- Broadening the Scope of Optimization using Partitioning -- Co-Optimization of Latches and Clock Networks -- Conclusions and Future Work.
Sommario/riassunto	This book introduces techniques that advance the capabilities and strength of modern software tools for physical synthesis, with the ultimate goal to improve the quality of leading-edge semiconductor products. It provides a comprehensive introduction to physical synthesis and takes the reader methodically from first principles

through state-of-the-art optimizations used in cutting edge industrial tools. It explains how to integrate chip optimizations in novel ways to create powerful circuit transformations that help satisfy performance requirements. Broadens the scope of physical synthesis optimization to include accurate transformations operating between the global and local scales; Integrates groups of related transformations to break circular dependencies and increase the number of circuit elements that can be jointly optimized to escape local minima; Derives several multi-objective optimizations from first observations through complete algorithms and experiments; Describes integrated optimization techniques that ensure a graceful timing closure process and impact nearly every aspect of a typical physical synthesis flow.