1. Record Nr. UNINA9910437959803321

Autore	Ben Abdallah Abderazek
Titolo	Multicore systems on-chip : practical software/hardware design / / Abderazek Ben Abdallah
Pubbl/distr/stampa	New York, : Springer, 2013
ISBN	94-91216-92-9
Edizione	[2nd ed.]
Descrizione fisica	1 online resource (xxvi, 273 pages) : illustrations (some color)
Collana	Atlantis ambient and pervasive intelligence ; ; v. 7
Disciplina	004.21 006.2 006.2/2
Soggetti	Systems on a chip Software architecture
Lingua di pubblicazione	Inglese
Formato	Materiale a stampa
Livello bibliografico	Monografia
Note generali	"ISSN: 1875-7669."
Nota di bibliografia	Includes bibliographical references.
Nota di contenuto	Introduction to Multicore Systems On-Chip -- Multicore SoCs Design Methods -- Multicore SoC Organization -- 2D Network-on-Chip -- 3D Network-on-Chip -- Network Interface Architecture and Design for 2D/3D NoCs -- Parallelizing Compiler for Single and Multicore Computing -- Power Optimization Techniques for Multicore SoCs -- Soft-Core Processor for Low-Power Embedded -- Dual-Execution Processor Architecture for Embedded -- Case Study: Deign of Embedded Multicore SoC.
Sommario/riassunto	System on chips designs have evolved from fairly simple unicore, single memory designs to complex heterogeneous multicore SoC architectures consisting of a large number of IP blocks on the same silicon. To meet high computational demands posed by latest consumer electronic devices, most current systems are based on such paradigm, which represents a real revolution in many aspects in computing. The attraction of multicore processing for power reduction is compelling. By splitting a set of tasks among multiple processor cores, the operating frequency necessary for each core can be reduced, allowing to reduce the voltage on each core. Because dynamic power is proportional to the frequency and to the square of the voltage, we get a big gain, even though we may have more cores running. As more and

more cores are integrated into these designs to share the ever increasing processing load, the main challenges lie in efficient memory hierarchy, scalable system interconnect, new programming paradigms, and efficient integration methodology for connecting such heterogeneous cores into a single system capable of leveraging their individual flexibility. Current design methods tend toward mixed HW/SW co-designs targeting multicore systems on-chip for specific applications. To decide on the lowest cost mix of cores, designers must iteratively map the device's functionality to a particular HW/SW partition and target architectures. In addition, to connect the heterogeneous cores, the architecture requires high performance complex communication architectures and efficient communication protocols, such as hierarchical bus, point-to-point connection, or Network-on-Chip. Software development also becomes far more complex due to the difficulties in breaking a single processing task into multiple parts that can be processed separately and then reassembled later. This reflects the fact that certain processor jobs cannot be easily parallelized to run concurrently on multiple processing cores and that load balancing between processing cores – especially heterogeneous cores – is very difficult.