1. Record Nr. UNINA9910437913103321

Autore	Czerwinski Robert
Titolo	Finite state machine logic synthesis for complex programmable logic devices / / Robert Czerwinski and Dariusz Kania
Pubbl/distr/stampa	Heidelberg [Germany] : , : Springer, , 2013
ISBN	3-642-36166-8
Edizione	[1st ed. 2013.]
Descrizione fisica	1 online resource (xiv, 172 pages) : illustrations
Collana	Lecture Notes in Electrical Engineering, , 1876-1100 ; ; 231
Disciplina	621.39/5 621.395
Soggetti	Programmable logic devices Sequential machine theory
Lingua di pubblicazione	Inglese
Formato	Materiale a stampa
Livello bibliografico	Monografia
Note generali	"ISSN: 1876-1100."
Nota di bibliografia	Includes bibliographical references and index.
Nota di contenuto	Introduction -- Definitions and Basic Properties -- Synthesis of FSMs -- State Assignment Algorithms -- Theoretical Background of Technology-Dependent Optimization -- The Algorithm of Area Optimization Based on Graphs of Outputs -- Conclusions -- Output File Format -- Conclusion.
Sommario/riassunto	This book is a monograph devoted to logic synthesis and optimization for CPLDs. CPLDs' macrocell can also be interpreted as programmable AND-fixed OR structure, well known as PAL-based structure. The question is: what should be done when the number of implicants representing function exceeds the number of product terms available in a logic block. The answer is ... in the book. Logic synthesis and optimization methods dedicated for PAL-based structures are proposed. The methods strive to find the optimum fit for the combinational logic and finite state machines to the structure of the logic device and aim at area and speed optimization. The theoretical background and complete strategies are richly illustrated with examples and figures.