1. Record Nr. UNINA9910437909903321

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Titolo	High-Performance D/A-Converters [[electronic resource]] : Application to Digital Transceivers / / by Martin Clara
Pubbl/distr/stampa	Berlin, Heidelberg : , : Springer Berlin Heidelberg : , : Imprint : Springer, , 2013
ISBN	1-283-94626-2 3-642-31229-2
Edizione	[1st ed. 2013.]
Descrizione fisica	1 online resource (296 p.)
Collana	Springer Series in Advanced Microelectronics, , 1437-0387 ; ; 36
Disciplina	621.38159
Soggetti	Signal processing Image processing Speech processing systems Electronics Microelectronics Semiconductors Electronic circuits Signal, Image and Speech Processing Electronics and Microelectronics, Instrumentation Electronic Circuits and Devices
Lingua di pubblicazione	Inglese
Formato	Materiale a stampa
Livello bibliografico	Monografia
Note generali	Description based upon print version of record.
Nota di bibliografia	Includes bibliographical references and index.
Nota di contenuto	Performance Figures of D/A-Converters -- Static Linearity -- Dynamic Linearity -- Noise-shaped D/A-Converters -- Advanced Current Calibration.
Sommario/riassunto	This book deals with modeling and implementation of high performance, current-steering D/A-converters for digital transceivers in nanometer CMOS technology. In the first part, the fundamental performance limitations of current-steering DACs are discussed. Based on simplified models, closed-form expressions for a number of basic non-ideal effects are derived and tested. With the knowledge of basic performance limits, the converter and system architecture can be optimized in an early design phase, trading off circuit complexity,

silicon area and power dissipation for static and dynamic performance. The second part describes four different current-steering DAC designs in standard 130 nm CMOS. The converters have a resolution in the range of 12-14 bits for an analog bandwidth between 2.2 MHz and 50 MHz and sampling rates from 100 MHz to 350 MHz. Dynamic-Element-Matching (DEM) and advanced dynamic current calibration techniques are employed to minimize the required silicon area.