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quantizer, the amplifier, and the switched capacitor network of the MDAC. Complementing the theoretical analyses of the various techniques, a power efficient operational transconductance amplifier is implemented and experimentally characterized. Furthermore, a medium-low resolution reference-free high-speed time-interleaved pipeline ADC employing all mentioned design techniques and circuits is presented, implemented and experimentally characterized. This ADC is said to be reference-free because it precludes any reference voltage, therefore saving power and area, as reference circuits are not necessary. Experimental results demonstrate the potential of the techniques which enabled the implementation of area and power efficient circuits. Describes various design techniques to enhance the power and area efficiency of building blocks for multiplying digital-toanalog converter (MDAC) based ADCs, such as Pipeline, Algorithmic, and multi-step Flash; Enables analog designers to enhance the performance of a range of circuits, without employing any type of digital assistance (calibration); Includes complete design flow of an ADC based on the proposed circuits and design techniques.