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Nota di bibliografia	Includes bibliographical references and index.
Nota di contenuto	Introduction -- Modeling and Specification of SoC Designs -- Automated Generation of Directed Tests -- Functional Test Compaction.- Property Clustering and Learning Techniques -- Decision Ordering Based Learning Techniques -- Synchronized Generation of Directed Tests -- Learning-Oriented Property Decomposition Approaches -- Directed Test Generation for Multicore Architectures -- Test Generation for Cache Coherence Validation.- Reuse of System-Level Tests for Implementation Validation -- Conclusion.
Sommario/riassunto	This book covers state-of-the art techniques for high-level modeling and validation of complex hardware/software systems, including those with multicore architectures. Readers will learn to avoid time-consuming and error-prone validation from the comprehensive coverage of system-level validation, including high-level modeling of designs and faults, automated generation of directed tests, and efficient validation methodology using directed tests and assertions. The methodologies described in this book will help designers to improve the quality of their validation, performing as much validation as possible in the early stages of the design, while reducing the overall validation effort and cost.