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Note generali	Includes index.
Nota di contenuto	Chapter 1. Introduction -- Chapter 2. Design Implementation Data Structures and Settings -- Chapter 3. Design Constraints Development -- Chapter 4. Multiple Modes and Multiple Corners Development -- Chapter 5. Concurrent Floor Planning and Placement -- Chapter 6. Placement and Timing Analysis -- Chapter 7. Clock Tree Synthesis and Timing Analysis -- Chapter 8. Detail Route and Timing, Power Analysis -- Chapter 9. Final Route and Timing Closure in all Modes and Corners -- Chapter 10. Functional and Physical Verification.
Sommario/riassunto	The Art of Timing Closure is written using a hands-on approach to describe advanced concepts and techniques using Multi-Mode Multi-Corner (MMMC) for an advanced ASIC design implementation. It focuses on the physical design, Static Timing Analysis (STA), formal and physical verification. The scripts in this book are based on Cadence® Encounter System™. However, if the reader uses a different EDA tool, that tool's commands are similar to those shown in this book. The topics covered are as follows: Data Structures Multi-Mode Multi-Corner

Analysis Design Constraints Floorplan and Timing Placement and Timing Clock Tree Synthesis Final Route and Timing Design Signoff

Rather than go into great technical depth, the author emphasizes short, clear descriptions which are implemented by references to authoritative manuscripts. It is the goal of this book to capture the essence of physical design and timing analysis at each stage of the physical design, and to show the reader that physical design and timing analysis engineering should be viewed as a single area of expertise. This book is intended for anyone who is involved in ASIC design implementation -- starting from physical design to final design signoff. Target audiences for this book are practicing ASIC design implementation engineers and students undertaking advanced courses in ASIC design. Provides readers with a hands-on, step-by-step approach to solving physical design and timing closure problems faced in designing for today's advanced technology nodes; Helps ASIC designers to be conversant with all aspects of ASIC design implementation stages including advance node device processes and libraries, place-and-route and verification; Enables improvement of so called "RTL-to-GDS" cycle time, by incorporating Multiple Mode Multiple Corner (MMMC) timing closure techniques in every step of physical design. .
