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Descrizione fisica	1 online resource (380 p.)
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Nota di bibliografia	Includes bibliographical references at the end of each chapters.
Nota di contenuto	Front Cover; Contents; Preface; Authors; Chapter 1: Introduction; Chapter 2: Interconnection Networks in Network-on-Chip; Chapter 3: Architecture Design of Network-on-Chip; Chapter 4: Evaluation of Network-on-Chip Architectures; Chapter 5: Application Mapping on Network-on-Chip; Chapter 6: Low-Power Techniques for Network-on-Chip; Chapter 7: Signal Integrity and Reliability of Network-on-Chip; Chapter 8: Testing of Network-on-Chip Architectures; Chapter 9: Application-Specific Network- on-Chip Synthesis; Chapter 10: Reconfigurable Network-on-Chip Design Chapter 11: Three-Dimensional Integration of Network-on-Chip Chapter 12: Conclusions and Future Trends; Back Cover
Sommario/riassunto	Addresses the Challenges Associated with System-on-Chip IntegrationNetwork-on-Chip: The Next Generation of System-on-Chip Integration examines the current issues restricting chip-on-chip communication efficiency, and explores Network-on-chip (NoC), a promising alternative that equips designers with the capability to produce a scalable, reusable, and high-performance communication backbone by allowing for the integration of a large number of cores on

a single system-on-chip (SoC). This book provides a basic overview of topics associated with NoC-based design: communication infrastructure design

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