1. Record Nr. UNINA9910409666503321

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Titolo	A Pipelined Multi-Core Machine with Operating System Support : Hardware Implementation and Correctness Proof / / by Petro Lutsyk, Jonas Oberhauser, Wolfgang J. Paul
Pubbl/distr/stampa	Cham : , : Springer International Publishing : , : Imprint : Springer, , 2020
ISBN	3-030-43243-2
Edizione	[1st ed. 2020.]
Descrizione fisica	1 online resource (634 pages)
Collana	Theoretical Computer Science and General Issues, , 2512-2029 ; ; 9999
Disciplina	005.434
Soggetti	Computer programming Computer engineering Computer networks Microprogramming Computer input-output equipment Logic programming Computer science Programming Techniques Computer Engineering and Networks Control Structures and Microprogramming Input/Output and Data Communications Logic in AI Theory of Computation
Lingua di pubblicazione	Inglese
Formato	Materiale a stampa
Livello bibliografico	Monografia
Nota di contenuto	Introductory material -- on hierarchical hardware design -- hardware library -- basic processor design -- pipelining -- cache memory systems -- interrupt mechanism -- self modification, instruction buffer and nondeterministic ISA -- memory management units -- store buffers -- multi-core processors -- advanced programmable interrupt controllers (APICs) -- adding a disk -- I/O apic.
Sommario/riassunto	This work is building on results from the book named “A Pipelined Multi-core MIPS Machine: Hardware Implementation and Correctness”

by M. Kovalev, S.M. Müller, and W.J. Paul, published as LNCS 9000 in 2014. It presents, at the gate level, construction and correctness proof of a multi-core machine with pipelined processors and extensive operating system support with the following features: • MIPS instruction set architecture (ISA) for application and for system programming • cache coherent memory system • store buffers in front of the data caches • interrupts and exceptions • memory management units (MMUs) • pipelined processors: the classical five-stage pipeline is extended by two pipeline stages for address translation • local interrupt controller (ICs) supporting inter-processor interrupts (IPIs) • I/O-interrupt controller and a disk .