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Nota di contenuto	Chapter 1: Introduction to FPGA design -- Chapter 2: Introduction to HDL -- Chapter 3:Introduction to SystemVerilog -- Chapter 4: Programming using SystemVerilog -- Chapter 5:Combinational design using SystemVerilog -- Chapter 6: Sequential design using SystemVerilog -- Chapter 7: RTL design using SystemVerilog -- Chapter 8: Verification using SystemVerilog -- Chapter 9: Design Implementation using FPGA.
Sommario/riassunto	This book introduces the reader to FPGA based design for RTL synthesis. It describes simple to complex RTL design scenarios using SystemVerilog. The book builds the story from basic fundamentals of FPGA based designs to advance RTL design and verification concepts using SystemVerilog. It provides practical information on the issues in the RTL design and verification and how to overcome these. It focuses on writing efficient RTL codes using SystemVerilog, covers design for the Xilinx FPGAs and also includes implementable code examples. The contents of this book cover improvement of design performance,

assertion based verification, verification planning, and architecture and system testing using FPGAs. The book can be used for classroom teaching or as a supplement in lab work for undergraduate and graduate coursework as well as for professional development and training programs. It will also be of interest to researchers and professionals interested in the RTL design for FPGA and ASIC.