1. Record Nr. UNINA9910403768303321

Autore	Goli Mehran
Titolo	Automated Analysis of Virtual Prototypes at the Electronic System Level : Design Understanding and Applications / / by Mehran Goli, Rolf Drechsler
Pubbl/distr/stampa	Cham : , : Springer International Publishing : , : Imprint : Springer, , 2020
ISBN	3-030-44282-9
Edizione	[1st ed. 2020.]
Descrizione fisica	1 online resource (XXI, 166 p. 53 illus.)
Disciplina	005.1028 620.0042
Soggetti	Electronic circuits Computer engineering Internet of things Embedded computer systems Microprocessors Circuits and Systems Cyber-physical systems, IoT Processor Architectures
Lingua di pubblicazione	Inglese
Formato	Materiale a stampa
Livello bibliografico	Monografia
Nota di contenuto	Chapter 1. Introduction -- Chapter 2. Background -- Chapter 3. Design Understanding Methodology -- Chapter 4. Application I: Verification -- Chapter 5. Application II: Security Validation -- Chapter 6. Application III: Design Space Exploration -- Chapter 7. Conclusion.
Sommario/riassunto	This book describes a set of SystemCbased virtual prototype analysis methodologies, including design understanding, verification, security validation, and design space exploration. Readers will gain an overview of the latest research results in the field of Electronic Design Automation (EDA) at the Electronic System Level (ESL). The methodologies discussed enable readers to tackle easily key tasks and applications in the design process. Provides an extensive introduction to the field of SystemCbased virtual prototype (VP) analysis at the electronic system level; Describes a design understanding methodology

from both debugger-based and compilerbased perspectives; Illustrates a semiformal verification approach to check the validity of a given VP against its specification, userdefined rules and protocol; Discusses a security validation approach to validate the runtime behavior of a given VP-based SoC against security threat models, such as information leakage (confidentiality) and unauthorized access to data in a memory (integrity); Describes a design space exploration approach for SystemC-based VPs to guide designers to know under which error limits, different portions of a given VP can be approximated at different granularity levels.