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Nota di contenuto	Introduction -- Practical Split Manufacturing Optimization -- IC Camouflaging Optimization and Evaluation -- Fault Attack Protection and Evaluation -- Conclusion.
Sommario/riassunto	This book proposes a synergistic framework to help IP vendors to protect hardware IP privacy and integrity from design, optimization, and evaluation perspectives. The proposed framework consists of five interacting components that directly target at the primary IP violations. All the five algorithms are developed based on rigorous mathematical modeling for primary IP violations and focus on different stages of IC design, which can be combined to provide a formal security guarantee.