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Titolo	Adaptive Digital Circuits for Power-Performance Range beyond Wide Voltage Scaling : From the Clock Path to the Data Path / / by Saurabh Jain, Longyang Lin, Massimo Alioto
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Descrizione fisica	1 online resource (XVI, 168 p. 113 illus., 107 illus. in color.)
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Nota di contenuto	Introduction to wide voltage scaling, applications and challenges -- Reconfigurable microarchitectures down to pipestage and memory bank level -- Automated design flows and run-time optimization for reconfigurable microarchitectures -- Case studies of reconfigurable microarchitectures: accelerators, microprocessors and memories -- Reconfigurable clock networks, automated design flows, run-time optimization and case study -- Conclusion.
Sommario/riassunto	This book offers the first comprehensive coverage of digital design techniques to expand the power-performance tradeoff well beyond that allowed by conventional wide voltage scaling. Compared to conventional fixed designs, the approach described in this book makes digital circuits more versatile and adaptive, allowing simultaneous optimization at both ends of the power-performance spectrum. Drop-in solutions for fully automated and low-effort design based on

commercial CAD tools are discussed extensively for processors, accelerators and on-chip memories, and are applicable to prominent applications (e.g., IoT, AI, wearables, biomedical). Through the higher power-performance versatility techniques described in this book, readers are enabled to reduce the design effort through reuse of the same digital design instance, across a wide range of applications. All concepts the authors discuss are demonstrated by dedicated testchip designs and experimental results. To make the results immediately usable by the reader, all the scripts necessary to create automated design flows based on commercial tools are provided and explained. Provides extensive coverage of the challenges and the key technologies enabling wide power-performance range in digital sub-systems (e.g., processors, memories, accelerators); Includes in-depth description of silicon-proven methodologies to design reconfigurable data path and clock path; Describes techniques for reconfigurable microarchitectures, down to the pipestage and the clock repeater level; Uses a highly interdisciplinary approach covering the circuit, the microarchitectural and the system levels of abstraction; Presents practical design examples and the related methodologies; Offers complementary design files and scripts, useful to replicate the presented developments and develop new designs.