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Nota di bibliografia	Includes bibliographical references and index.
Nota di contenuto	Introduction -- Automatic Generation of Cycle-Accurate Simulink Blocks from HDL IPs -- Towards Early Validation of Firmware-Based Power Management Using Virtual Prototypes: A Constrained Random Approach -- Symbolic Simulation of Dataflow Synchronous Programs with Timers -- Language and Hardware Acceleration Backend for Graph Processing -- Runtime Task Mapping for Lifetime Budgeting in Many-Core Systems -- Fault Analysis in Analog Circuits through Language Manipulation and Abstraction -- Towards Consistency Checking Between HDL and UPF Descriptions.
Sommario/riassunto	This book brings together a selection of the best papers from the twenty-first edition of the Forum on specification and Design Languages Conference (FDL), which took place on September 10-12, 2018, in Munich, Germany. FDL is a well-established international forum devoted to dissemination of research results, practical experiences and new ideas in the application of specification, design

and verification languages to the design, modeling and verification of integrated circuits, complex hardware/software embedded systems, and mixed-technology systems. Covers Assertion Based Design, Verification & Debug; Includes language-based modeling and design techniques for embedded systems; Covers design, modeling and verification of mixed physical domain and mixed signal systems that include significant analog parts in electrical and non-electrical domains; Includes formal and semi-formal system level design methods for complex embedded systems based on the Unified Modelling Language (UML) and Model Driven Engineering (MDE).