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Titolo	Trustworthy Hardware Design: Combinational Logic Locking Techniques // by Muhammad Yasin, Jeyavijayan (JV) Rajendran, Ozgur Sinanoglu
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Collana	Analog Circuits and Signal Processing, , 1872-082X
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Soggetti	Electronic circuits Logic design Computer arithmetic and logic units Circuits and Systems Logic Design Arithmetic and Logic Structures
Lingua di pubblicazione	Inglese
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Livello bibliografico	Monografia
Nota di contenuto	The Need for Logic Locking -- A Brief History of Logic Locking -- Pre-SAT Logic Locking -- The SAT Attack -- Post-SAT 1: Point function-based Logic Locking -- Approximate Attacks -- Structural Attacks -- Post-SAT 2: Insertion of SAT-unresolvable Structures -- Post-SAT 3: Stripped-Functionality Logic Locking.
Sommario/riassunto	With the popularity of hardware security research, several edited monograms have been published, which aim at summarizing the research in a particular field. Typically, each book chapter is a recompilation of one or more research papers, and the focus is on summarizing the state-of-the-art research. Different from the edited monograms, the chapters in this book are not re-compilations of research papers. The book follows a pedagogical approach. Each chapter has been planned to emphasize the fundamental principles behind the logic locking algorithms and relate concepts to each other using a systematization of knowledge approach. Furthermore, the authors of this book are in a good position to be able to deliver such a

book, as they contributed to this field significantly through numerous fundamental papers.
