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| Autore | Shirinzadeh Saeideh |
| Titolo | In-Memory Computing [[electronic resource] ] : Synthesis and Optimization / / by Saeideh Shirinzadeh, Rolf Drechsler |
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| Descrizione fisica | 1 online resource (121 pages) : illustrations |
| Disciplina | 004.5 |
| Soggetti | Electronic circuits<br>Microprocessors<br>Electronics<br>Microelectronics<br>Circuits and Systems<br>Processor Architectures<br>Electronics and Microelectronics, Instrumentation |
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| Livello bibliografico | Monografia |
| Nota di bibliografia | Includes bibliographical references and index. |
| Nota di contenuto | Chapter 1: Introduction -- Chapter 2: Background -- Chapter 3: BDD Optimization and Approximation: A Multi-Criteria Approach -- Chapter 4: Synthesis for Logic-in-Memory Computing using RRAM -- Chapter 5: Compilation and Wear Le0veling for Programmable Logic-in-Memory (PLiM) Architecture -- Chapter 6: Conclusions. |
| Sommario/riassunto | This book describes a comprehensive approach for synthesis and optimization of logic-in-memory computing hardware and architectures using memristive devices, which creates a firm foundation for practical applications. Readers will get familiar with a new generation of computer architectures that potentially can perform faster, as the necessity for communication between the processor and memory is surpassed. The discussion includes various synthesis methodologies and optimization algorithms targeting implementation cost metrics including latency and area overhead as well as the reliability issue caused by short memory lifetime. Presents a comprehensive synthesis flow for the emerging field of logic-in- |

memory computing; Describes automated compilation of programmable logic-in-memory computer architectures; Includes several effective optimization algorithm also applicable to classical logic synthesis; Investigates unbalanced write traffic in logic-in-memory architectures and describes wear leveling approaches to alleviate it.