1. Record Nr. UNINA9910366582703321

Autore	Mehta Ashok B.
Titolo	System Verilog Assertions and Functional Coverage : Guide to Language, Methodology and Applications / / by Ashok B. Mehta
Pubbl/distr/stampa	Cham : , : Springer International Publishing : , : Imprint : Springer, , 2020
ISBN	3-030-24737-6
Edizione	[3rd ed. 2020.]
Descrizione fisica	1 online resource (XXXIX, 507 p. 270 illus., 258 illus. in color.)
Disciplina	621.3815 621.392
Soggetti	Electronic circuits Electronics Microelectronics Microprocessors Circuits and Systems Electronics and Microelectronics, Instrumentation Processor Architectures
Lingua di pubblicazione	Inglese
Formato	Materiale a stampa
Livello bibliografico	Monografia
Note generali	Includes index.
Nota di contenuto	Introduction -- System Verilog Assertions -- Immediate Assertions -- Concurrent Assertions – Basics (sequence, property, assert) -- Sampled Value Functions $rose, $fell -- Operators -- System Functions and Tasks -- Multiple clocks -- Local Variables -- Recursive property -- Detecting and using endpoint of a sequence -- ‘expect’ -- ‘assume’ and formal (static functional) verification -- Other important topics -- Asynchronous Assertions !!! -- IEEE-1800–2009 Features -- SystemVerilog Assertions LABs -- System Verilog Assertions – LAB Answers -- Functional Coverage -- Performance Implications of coverage methodology -- Coverage Options.
Sommario/riassunto	This book provides a hands-on, application-oriented guide to the language and methodology of both SystemVerilog Assertions and Functional Coverage. Readers will benefit from the step-by-step approach to learning language and methodology nuances of both SystemVerilog Assertions and Functional Coverage, which will enable

them to uncover hidden and hard to find bugs, point directly to the source of the bug, provide for a clean and easy way to model complex timing checks and objectively answer the question ‘have we functionally verified everything’. Written by a professional end-user of ASIC/SoC/CPU and FPGA design and Verification, this book explains each concept with easy to understand examples, simulation logs and applications derived from real projects. Readers will be empowered to tackle the modeling of complex checkers for functional verification and exhaustive coverage models for functional coverage, thereby drastically reducing their time to design, debug and cover. This updated third edition addresses the latest functional set released in IEEE-1800 (2012) LRM, including numerous additional operators and features. Additionally, many of the Concurrent Assertions/Operators explanations are enhanced, with the addition of more examples and figures. · Covers in its entirety the latest IEEE-1800 2012 LRM syntax and semantics; · Covers both SystemVerilog Assertions and SystemVerilog Functional Coverage languages and methodologies; · Provides practical applications of the what, how and why of Assertion Based Verification and Functional Coverage methodologies; · Explains each concept in a step-by-step fashion and applies it to a practical real life example; · Includes 6 practical LABs that enable readers to put in practice the concepts explained in the book.