1. Record Nr. UNINA9910366580003321

Autore	Manna Kanchan
Titolo	Design and Test Strategies for 2D/3D Integration for NoC-based Multicore Architectures [[electronic resource] /] / by Kanchan Manna, Jimson Mathew
Pubbl/distr/stampa	Cham : , : Springer International Publishing : , : Imprint : Springer, , 2020
ISBN	3-030-31310-7
Edizione	[1st ed. 2020.]
Descrizione fisica	1 online resource
Disciplina	621.381531
Soggetti	Electronic circuits Microprocessors Electronics Microelectronics Circuits and Systems Processor Architectures Electronics and Microelectronics, Instrumentation
Lingua di pubblicazione	Inglese
Formato	Materiale a stampa
Livello bibliografico	Monografia
Nota di bibliografia	Includes bibliographical references and index.
Nota di contenuto	Introduction to Network-on-Chip Designs and Tests -- Iterative Mapping with Through Silicon Via (TSV) placement for 3D-NoC-based multicore systems -- A constructive Heuristic for integrated mapping and TSV Placement for 3D-NoC-based multicore systems -- Discrete Particle Swarm Optimization for integrated mapping and TSV Placement for 3D-NoC-based multicore systems -- Temperature-aware application mapping strategy for 2D-NoC-based multicore systems -- Temperature-aware design strategy for 3D-NoC-based multicore systems -- Temperature-aware test strategy for 2D as well as 3D-NoC-based multicore systems.
Sommario/riassunto	This book covers various aspects of optimization in design and testing of Network-on-Chip (NoC) based multicore systems. It gives a complete account of the state-of-the-art and emerging techniques for near optimal mapping and test scheduling for NoC-based multicores. The authors describe the use of the Integer Line Programming (ILP)

technique for smaller benchmarks and a Particle Swarm Optimization (PSO) to get a near optimal mapping and test schedule for bigger benchmarks. The PSO-based approach is also augmented with several innovative techniques to get the best possible solution. The tradeoff between performance (communication or test time) of the system and thermal-safety is also discussed, based on designer specifications. Provides a single-source reference to design and test for circuit and system-level approaches to (NoC) based multicore systems; Gives a complete account of the state-of-the-art and emerging techniques for near optimal mapping and test scheduling in (NoC) based multicore systems; Organizes chapters systematically and hierarchically, rather than in an ad hoc manner, covering aspects of optimization in design and testing of Network-on-Chip (NoC) based multicore systems.