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   Sommario/riassunto   This book introduces readers to a reconfigurable chip architecture for future wireless communication systems, such as 5G and beyond. The proposed architecture perfectly meets the demands for future mobile communication solutions to support different standards, algorithms, and antenna sizes, and to accommodate the evolution of standards and algorithms. It employs massive MIMO detection algorithms, which combine the advantages of low complexity and high parallelism, and can fully meet the requirements for detection accuracy. Further, the architecture is implemented using ASIC, which offers high energy efficiency, high area efficiency and low detection error. After introducing massive MIMO detection algorithms and circuit architectures, the book describes the ASIC implementation for verifying the massive MIMO detection. In turn, it provides detailed information on the proposed reconfigurable architecture: the data path and configuration path for massive MIMO detection algorithms, including the processing unit, interconnections, storage mechanism, configuration information format, and configuration method. .