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Sommario/riassunto	This thesis presents the SiGe source and drain (S/D) technology in the context of advanced CMOS, and addresses both device processing and epitaxy modelling. As the CMOS technology roadmap calls for continuously downscaling traditional transistor structures, controlling the parasitic effects of transistors, e.g. short channel effect, parasitic resistances and capacitances is becoming increasingly difficult. The emergence of these problems sparked a technological revolution, where a transition from planar to three-dimensional (3D) transistor design occurred in the 22nm technology node. The selective epitaxial growth (SEG) method has been used to deposit SiGe as stressor material in S/D regions to induce uniaxial strain in the channel region. The thesis investigates issues of process integration in IC production and concentrates on the key parameters of high-quality SiGe selective

epitaxial growth, with a special focus on its pattern dependency behavior and on key integration issues in both 2D and 3D transistor structures, the goal being to improve future applications of SiGe SEG in advanced CMOS.
