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Nota di contenuto	Machine Learning and Neural Networks -- Approximate FPGA-based LSTMs under Computation Time Constraints -- Redundancy-reduced MobileNet Acceleration on Reconfigurable Logic For ImageNet Classification -- Accuracy to Throughput Trade-offs for Reduced Precision Neural Networks on Reconfigurable Logic -- Deep Learning on High Performance FPGA Switching Boards: Flow-in-Cloud -- SqueezeJet: High-level Synthesis Accelerator Design for Deep Convolutional Neural Networks -- Efficient hardware acceleration of

recommendation engines: a use case on collaborative filtering -- FPGA-based Design and CGRA Optimizations -- VerCoLib: Fast and Versatile Communication for FPGAs via PCI Express -- Performance Estimation of FPGA Modules for Modular Design Methodology using Artificial Neural Network -- Achieving Efficient Realization of Kalman Filter on CGRA through Algorithm-Architecture Co-design -- FPGA-based Memory Efficient Shift-And Algorithm for Regular Expression Matching -- Towards an optimized multi FPGA architecture with STDM network: a preliminary study -- Applications and Surveys -- An FPGA/HMC-based Accelerator for Resolution Proof Checking -- An Efficient FPGA Implementation of the Big Bang-Big Crunch Optimization Algorithm -- ReneGENE-GI: Empowering Precision Genomics with FPGAs on HPCs.-FPGA-based Parallel Pattern Matching -- Embedded Vision Systems: A Review of the Literature -- A Survey of Low Power Design Techniques for Last Level Caches -- Fault-Tolerance, Security and Communication Architectures -- ISA-DTMR: Selective Protection in Configurable Heterogeneous Multicores -- Analyzing AXI Streaming Interface for Hardware Acceleration in AP-SoC under Soft Errors -- High Performance UDP/IP 40Gb Ethernet Stack for FPGAs -- Tackling Wireless Sensor Network Heterogeneity Through Novel Reconfigurable Gateway Approach -- A Low-Power FPGA-Based Architecture for Microphone Arrays in Wireless Sensor Networks -- A Hybrid FPGA Trojan Detection Technique Based-on Combinatorial Testing and On-chip Sensing -- HoneyWiN: Novel Honeycomb-based Wireless NoC Architecture in Many-Core Era -- Reconfigurable and Adaptive Architectures -- Fast Partial Reconfiguration on SRAM-based FPGAs: A Frame-Driven Routing Approach -- A Dynamic Partial Reconfigurable Overlay Framework for Python -- Runtime Adaptive Cache for the LEON3 Processor -- Exploiting Partial Reconfiguration on a Dynamic Coarse Grained Reconfigurable Architecture -- DIM-VEX: Exploiting Design Time Configurability and Runtime Reconfigurability -- The use of HACP+SBT lossless compression in optimizing memory bandwidth requirement for hardware implementation of background modelling algorithms -- A Reconfigurable PID Controller -- Design Methods and Fast Prototyping -- High-Level Synthesis of Software-defined MPSoCs -- Improved High-Level Synthesis for Complex CellML Models -- An Intrusive Dynamic Reconfigurable Cycle-accurate Debugging System for Embedded Processors -- Rapid prototyping and verification of hardware modules generated using HLS -- Comparing C and SystemC Based HLS Methods for Reconfigurable Systems Design -- Fast DSE for Automated Parallelization of Embedded Legacy Applications -- Control Flow Analysis for Embedded Multi-Core Hybrid Systems -- FPGA-based Design and Applications -- A Low-Cost BRAM-based Function Reuse for Configurable Soft-Core Processors in FPGAs -- A Parallel-Pipelined OFDM Baseband Modulator with Dynamic Frequency Scaling for 5G Systems -- Area-Energy Aware Dataow Optimisation of Visual Tracking Systems -- Fast Carry Chain based Architectures for Two's Complement to CSD Recoding on FPGAs -- Exploring Functional Acceleration of OpenCL on FPGAs and GPUs Through Platform-Independent Optimizations -- ReneGENE-Novo: Co-designed Algorithm-Architecture for Accelerated Preprocessing and Assembly of Genomic Short Reads -- An OpenCL Implementation of WebP Accelerator on FPGAs -- Efficient Multitasking on FPGA Using HDL-based Checkpointing -- High Level Synthesis Implementation of Object Tracking Algorithm on Reconfigurable Hardware -- Reconfigurable FPGA-Based Channelization Using Polyphase Filter Banks for Quantum Computing Systems -- Reconfigurable IP-Based Spectral Interference Canceller -- FPGA-Assisted Distribution Grid Simulator -- Analyzing

the Use of Taylor Series Approximation in Hardware and Embedded Software for Good Cost-Accuracy Tradeoffs -- Special Session: Research Projects -- CGRA Tool Flow for Fast Run-Time Reconfiguration -- Seamless FPGA deployment over Spark in cloud computing: A use case on Machine learning hardware acceleration -- The ARAMiS Project Initiative: Multicore Systems in Safety- and Mixed-Critical Applications -- Mapping and scheduling hard real time applications on multicore systems - The ARGO approach -- Robots in assisted living environments as an unobtrusive, efficient, reliable and modular solution for independent ageing: The RADIO Experience -- HLS Algorithmic Explorations for HPC Execution on Reconfigurable Hardware ECOSCALE -- Supporting uTilities for Heterogeneous EMbedded image processing platforms (STHEM): An Overview.

Sommario/riassunto

This book constitutes the proceedings of the 14th International Conference on Applied Reconfigurable Computing, ARC 2018, held in Santorini, Greece, in May 2018. The 29 full papers and 22 short presented in this volume were carefully reviewed and selected from 78 submissions. In addition, the volume contains 9 contributions from research projects. The papers were organized in topical sections named: machine learning and neural networks; FPGA-based design and CGRA optimizations; applications and surveys; fault-tolerance, security and communication architectures; reconfigurable and adaptive architectures; design methods and fast prototyping; FPGA-based design and applications; and special session: research projects. .