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Titolo	62142-2005 - IEC/IEEE iInternational standard - Verilog(R) Register Transfer Level synthesis / / Institute of Electrical and Electronics Engineers
Pubbl/distr/stampa	New York, New York : , : IEEE, , 2002
ISBN	0-7381-4777-X
Descrizione fisica	1 online resource (116 pages)
Disciplina	621.392
Soggetti	VHDL (Computer hardware description language)
Lingua di pubblicazione	Inglese
Formato	Materiale a stampa
Livello bibliografico	Monografia
Sommario/riassunto	Replaces IEEE Std 1364.1-2002. To develop a standard syntax and semantics for Verilog RTL synthesis. This standard shall define the subset of IEEE 1364 (Verilog HDL) which is suitable for RTL synthesis and shall define the semantics of that subset for the synthesis domain. This standard shall be based on the current existing standard IEEE 1364.