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Soggetti	Computer networks Operating systems (Computers) Logic design Computer systems Computer input-output equipment Microprocessors Computer architecture Computer Communication Networks Operating Systems Logic Design Computer System Implementation Input/Output and Data Communications Processor Architectures
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Nota di contenuto	Dependable Systems -- Hardware/Software Co-designed Security Extensions for Embedded Devices -- SDES - Scalable Software Support for Dependable Embedded Systems -- Real-Time Systems -- Asynchronous Critical Sections in Real-Time Multiprocessor Systems -- Resource-Aware Parameter Tuning for Real-Time Applications -- A Hybrid NoC Enabling Fail-Operational and Hard Real-Time

Communication in MPSoC -- Special Applications -- DSL-based Acceleration of Automotive Environment Perception and Mapping Algorithms for embedded CPUs, GPUs, and FPGAs -- Applying the Concept of Artificial DNA and Hormone System to a Low-Performance Automotive Environment -- A Parallel Adaptive Swarm Search Framework for Solving Black-Box Optimization Problems -- Architecture -- Leros: the Return of the Accumulator Machine -- A Generic Functional Simulation of Heterogeneous Systems -- Evaluating Dynamic Task Scheduling in a Task-based Runtime System for Heterogeneous Architectures -- Dynamic Scheduling of Pipelined Functional Units in Coarse-Grained Reconfigurable Array Elements -- Memory Hierarchy -- CyPhOS { A Component-based Cache-Aware Multi-Core Operating System -- Investigation of L2-Cache interferences in a NXP QorIQ T4240 multicore processor -- MEMPower: Data-Aware GPU Memory Power Model -- FPGA -- Effective FPGA Architecture for General CRC -- Receive-Side Notification for Enhanced RDMA in FPGA Based Networks -- An Efficient FPGA Accelerator Design for Optimized CNNs using OpenCL -- Energy Awareness -- The Return of Power Gating: Smart Leakage Energy Reductions in Modern Out-of-Order Processor Architectures -- A Heterogeneous and Reconfigurable Embedded Architecture for Energy-efficient Execution of Convolutional Neural Networks -- An energy efficient embedded processor for hard real-time Java applications -- NoC/SoC -- A Minimal Network Interface for a Simple Network-on-Chip -- Network Coding in Networks-on-Chip with Lossy Links -- Application Specific Reconfigurable SoC Interconnection Network Architectures.

Sommario/riassunto

This book constitutes the proceedings of the 32nd International Conference on Architecture of Computing Systems, ARCS 2019, held in Copenhagen, Denmark, in May 2019. The 24 full papers presented in this volume were carefully reviewed and selected from 40 submissions. ARCS has always been a conference attracting leading-edge research outcomes in Computer Architecture and Operating Systems, including a wide spectrum of topics ranging from embedded and real-time systems all the way to large-scale and parallel systems. The selected papers are organized in the following topical sections: Dependable systems; real-time systems; special applications; architecture; memory hierarchy; FPGA; energy awareness; NoC/SoC. The chapter 'MEMPower: Data-Aware GPU Memory Power Model' is open access under a CC BY 4.0 license at link.springer.com.