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Nota di contenuto	Part 1. Introduction -- Post-Silicon SoC Validation Challenges -- Part 2. Debug Infrastructure -- SoC Instrumentations: Pre-silicon Preparation for Post-silicon Readiness -- Structure-based Signal Selection for Post-silicon Validation -- Simulation-based Signal Selection -- Hybrid Signal Selection -- Post-Silicon Signal Selection using Machine Learning -- Part 3. Generation of Tests and Assertions -- Observability-aware Post-Silicon Test Generation -- On-chip Constrained-Random Stimuli Generation -- Test Generation and Lightweight Checking for Multi-core Memory Consistency -- Selection of Post-Silicon Hardware Assertions -- Part 4. Post-Silicon Debug -- Debug Data Reduction Techniques -- High-level Debugging of Post-silicon Failures -- Post-silicon Fault Localization with Satisfiability Solvers -- Coverage Evaluation and Analysis of Post-silicon Tests with Virtual Prototypes -- Utilization of Debug Infrastructure for Post-Silicon Coverage Analysis -- Part 5. Case Studies -- Network-on-Chip Validation and Debug -- Post-silicon Validation of the IBM Power8 Processor -- Part 6. Conclusion and

	Future Directions -- SoC Security versus Post-Silicon Debug Conflict -- The Future of Post-Silicon Debug.
Sommario/riassunto	This book provides a comprehensive coverage of System-on-Chip (SoC) post-silicon validation and debug challenges and state-of-the-art solutions with contributions from SoC designers, academic researchers as well as SoC verification experts. The readers will get a clear understanding of the existing debug infrastructure and how they can be effectively utilized to verify and debug SoCs. Provides a comprehensive overview of the SoC post-silicon validation and debug challenges; Covers state-of-the-art techniques for developing on-chip debug infrastructure; Describes automated techniques for generating post-silicon tests and assertions to enable effective post-silicon debug and coverage analysis; Covers scalable post-silicon validation and bug localization using a combination of simulation-based techniques and formal methods; Presents case studies for post-silicon debug of industrial SoC designs.