1. Record Nr. UNINA9910703571903321

Autore	Lewan M. D (Michael D.), <1948->
Titolo	Gas : oil ratios for source rocks containing Type-I, -II, -IIS, and -III kerogens as determined by hydrous pyrolysis / / by Michael D. Lewan and Allison A. Henry
Pubbl/distr/stampa	[Reston, Va.?] : , : U.S. Department of the Interior, U.S. Geological Survey, , [1999]
Descrizione fisica	1 online resource (17 pages) : illustrations
Collana	Open file report ; ; 99-327
Soggetti	Kerogen Natural gas Petroleum
Lingua di pubblicazione	Inglese
Formato	Materiale a stampa
Livello bibliografico	Monografia
Note generali	Title from title screen (viewed on Jan. 30, 2015).
Nota di bibliografia	Includes bibliographical references (pages 8-10).

2. Record Nr. UNINA9910337620903321

Autore	Taraate Vaibbhav
Titolo	Advanced HDL Synthesis and SOC Prototyping : RTL Design Using Verilog / / by Vaibbhav Taraate
Pubbl/distr/stampa	Singapore : , : Springer Singapore : , : Imprint : Springer, , 2019
ISBN	981-10-8776-8
Edizione	[1st ed. 2019.]
Descrizione fisica	1 online resource (xxi, 307 pages)
Disciplina	621.3815
Soggetti	Electronic circuits Microprogramming Logic design Circuits and Systems Control Structures and Microprogramming Logic Design
Lingua di pubblicazione	Inglese
Formato	Materiale a stampa
Livello bibliografico	Monografia
Nota di contenuto	Introduction -- SOC Design -- RTL Design Guidelines -- RTL Design and Verification -- Processor cores and Architecture design -- Buses and protocols in SOC designs -- DSP Algorithms and Video Processing -- ASIC and FPGA Synthesis -- Static Timing Analysis -- SOC Prototyping -- SOC Prototyping guidelines -- Design Integration and SOC synthesis -- Interconnect delays and Timing -- SOC Prototyping and debug techniques -- Testing at the board level.
Sommario/riassunto	This book describes RTL design using Verilog, synthesis and timing closure for System On Chip (SOC) design blocks. It covers the complex RTL design scenarios and challenges for SOC designs and provides practical information on performance improvements in SOC, as well as Application Specific Integrated Circuit (ASIC) designs. Prototyping using modern high density Field Programmable Gate Arrays (FPGAs) is discussed in this book with the practical examples and case studies. The book discusses SOC design, performance improvement techniques, testing and system level verification, while also describing the modern Intel FPGA/XILINX FPGA architectures and their use in SOC prototyping. Further, the book covers the Synopsys Design Compiler (DC) and Prime

Time (PT) commands, and how they can be used to optimize complex ASIC/SOC designs. The contents of this book will be useful to students and professionals alike.