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Nota di contenuto	1. Automatic Integration of HDL IPs in Simulink using FMI and S-Function Interfaces -- 2. Towards Early Validation of Firmware-Based Power Management using Virtual Prototypes: A Constrained Random Approach -- 3. Symbolic Simulation of Dataflow Synchronous Programs with Timers -- 4. Language and Hardware Acceleration Backend for Graph Processing -- 5. Fault Analysis in Analog Circuits through Language Manipulation and Abstraction -- 6. A Methodology for Automated Consistency Checking Between Different Power-Aware Descriptions.
Sommario/riassunto	This book brings together a selection of the best papers from the twentieth edition of the Forum on Specification and Design Languages Conference (FDL), which took place on September 18-20, 2017, in Verona, Italy. FDL is a well-established international forum devoted to dissemination of research results, practical experiences and new ideas

in the application of specification, design and verification languages to the design, modeling and verification of integrated circuits, complex hardware/software embedded systems, and mixed-technology systems. Covers modeling and verification methodologies targeting digital and analog systems; Addresses firmware development and validation; Targets both functional and non-functional properties; Includes descriptions of methods for reliable system design.

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