Record Nr. UNINA9910299951203321 Autore Champac Victor Titolo Timing Performance of Nanometer Digital Circuits Under Process Variations / / by Victor Champac, Jose Garcia Gervacio Pubbl/distr/stampa Cham: .: Springer International Publishing: .: Imprint: Springer. . 2018 **ISBN** 3-319-75465-3 Edizione [1st ed. 2018.] Descrizione fisica 1 online resource (195 pages) Collana Frontiers in Electronic Testing, , 0929-1296;; 39 Disciplina 621.381 Soggetti Electronic circuits Microprocessors Electronics Microelectronics Circuits and Systems **Processor Architectures** Electronics and Microelectronics, Instrumentation Lingua di pubblicazione Inglese **Formato** Materiale a stampa Livello bibliografico Monografia Nota di contenuto Introduction -- Mathematical Fundamentals -- Process Variations --Gate delay under process variations -- Path Delay Under Process Variations -- Circuit Analysis under Process Variations -- FinFET Technology and design issues. This book discusses the digital design of integrated circuits under Sommario/riassunto process variations, with a focus on design-time solutions. The authors describe a step-by-step methodology, going from logic gates to logic paths to the circuit level. Topics are presented in comprehensively, without overwhelming use of analytical formulations. Emphasis is placed on providing digital designers with understanding of the sources of process variations, their impact on circuit performance and tools for improving their designs to comply with product specifications. Various circuit-level "design hints" are highlighted, so that readers can use then to improve their designs. A special treatment is devoted to

unique design issues and the impact of process variations on the performance of FinFET based circuits. This book enables readers to

make optimal decisions at design time, toward more efficient circuits, with better yield and higher reliability.