1. Record Nr. UNINA9910299911803321

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Titolo	ASIC/SoC Functional Design Verification : A Comprehensive Guide to Technologies and Methodologies / / by Ashok B. Mehta
Pubbl/distr/stampa	Cham : , : Springer International Publishing : , : Imprint : Springer, , 2018
ISBN	3-319-59418-4
Edizione	[1st ed. 2018.]
Descrizione fisica	1 online resource (XXXI, 328 p. 175 illus., 160 illus. in color.)
Disciplina	621.3815
Soggetti	Electronic circuits Microprocessors Logic design Circuits and Systems Processor Architectures Logic Design
Lingua di pubblicazione	Inglese
Formato	Materiale a stampa
Livello bibliografico	Monografia
Nota di contenuto	Chapter 1.Introduction -- Chapter 2.Functional Verification-Challeenges and Solution -- Chapter 3.SystemVerilog Paradigm -- Chapter 4. UVM -- Chapter 5.CRV -- Chapter 6.SVA -- Chapter 7.SFC -- Chapter 8.CDC -- Chapter 9.Low Power Verification -- Chapter 10. Static Verification -- Chapter 11.ESL -- Chapter 12. Hardware/Software Co-verification -- Chapter 13 -- Analog Mixed Signals Verification -- Chapter 14 -- SOC Interconnect Verification -- Chapter 15. The Complete Product Design Lifecycle -- Chapter 16. Voice Over IP -- Chapter 17. Cache Memory Subsystem Verification: UVM Agent Based -- Chapter 18. Cache Memory Subsystem Verification: ISS Based.
Sommario/riassunto	This book describes in detail all required technologies and methodologies needed to create a comprehensive, functional design verification strategy and environment to tackle the toughest job of guaranteeing first-pass working silicon The author outlines all of the verification sub-fields at a high level, with just enough depth to allow a manager/decision maker or an engineer to grasp the field which can then be pursued in detail with the provided references. He describes in

detail industry standard technologies such as UVM (Universal Verification Methodology), SVA (SystemVerilog Assertions), SFC (SystemVerilog Functional Coverage), CDV (Coverage Driven Verification), Low Power Verification (Unified Power Format UPF), AMS (Analog Mixed Signal) verification, Virtual Platform TLM2.0/ESL (Electronic System Level) methodology, Static Formal Verification, Logic Equivalency Check (LEC), Hardware Acceleration, Hardware Emulation, Hardware/Software Co-verification, Power Performance Area (PPA) analysis on a virtual platform, Reuse Methodology from Algorithm/ESL to RTL, and other overall methodologies.