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Note generali	Description based upon print version of record.
Nota di contenuto	Introduction -- Analysis of Quantization Noise Reduction Techniques for Fractional-N PLL -- A Wide-Band 0.13 μ m SiGe BiCMOS PLL for X-Band Radar -- Design and Analysis of QVCO with Different Coupling Techniques -- Design and Analysis of a 0.6V QVCO with Capacitive-Coupling Technique -- Conclusions.
Sommario/riassunto	This book introduces low-noise and low-power design techniques for phase-locked loops and their building blocks. It summarizes the noise reduction techniques for fractional-N PLL design and introduces a novel capacitive-quadrature coupling technique for multi-phase signal generation. The capacitive-coupling technique has been validated

through silicon implementation and can provide low phase-noise and accurate I-Q phase matching, with low power consumption from a super low supply voltage. Readers will be enabled to pick one of the most suitable QVCO circuit structures for their own designs, without additional effort to look for the optimal circuit structure and device parameters. .
