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Titolo	Wafer-Level Chip-Scale Packaging : Analog and Power Semiconductor Applications // by Shichun Qu, Yong Liu
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Nota di bibliografia	Includes bibliographical references and index.
Nota di contenuto	Chapter 1. Demand and Challenges for Wafer Level Analog and Power Packaging -- Chapter 2. Fan-In Analog Wafer Level Chip Scale Package -- Chapter 3. Fan-Out Analog Wafer Level Chip Scale Package -- Chapter 4. Wafer Level Analog Chip Scale Package Stackable Design -- Chapter 5. Wafer Level Discrete Power MOSFET Package Design -- Chapter 6. Wafer Level Packaging TSV/Stack die for Integration of Analog and Power Solution -- Chapter 7. Thermal Management, Design, Analysis for WLCSP -- Chapter 8. Electrical and Multi-Physics Simulations for Analog and Power WLCSP -- Chapter 9. WLCSP Typical Assembly Process -- Chapter 10. WLCSP Typical Reliability and Test.

This book presents a state-of-art and in-depth overview in analog and power WLCSP design, material characterization, reliability, and modeling. Recent advances in analog and power electronic WLCSP packaging are presented based on the development of analog technology and power device integration. The book covers in detail how advances in semiconductor content, analog and power advanced WLCSP design, assembly, materials, and reliability have co-enabled significant advances in fan-in and fan-out with redistributed layer (RDL) of analog and power device capability during recent years. Along with new analog and power WLCSP development, the role of modeling is a key to assure successful package design. An overview of the analog and power WLCSP modeling and typical thermal, electrical, and stress modeling methodologies is also provided. This book also:

- Covers the development of wafer-level power discrete packaging with regular wafer-level design concepts and directly bumping technology
- Introduces the development of the analog and power SIP/3D/TSV/stack die packaging technology
- Presents the wafer-level analog IC packaging design through fan-in and fan-out with RDLs.
