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	Nota di contenuto	Introduction -- Preliminaries -- Part I Debug of Design Bugs -- Automated Debugging for Logic Bugs -- Automated Debugging from Pre-Silicon to Post-Silicon -- Automated Debugging for Synchronization Bugs -- Part II Debug of Delay Faults -- Analyzing Timing Variations -- Automated Debugging for Timing Variations -- Efficient Automated Speedpath Debugging -- Part III Debug of Transactions -- Online Debug for NoC-Based Multiprocessor SoCs -- Summary and Outlook.
	Sommario/riassunto	This book describes automated debugging approaches for the bugs and the faults which appear in different abstraction levels of a hardware system. The authors employ a transaction-based debug approach to systems at the transaction-level, asserting the correct relation of transactions. The automated debug approach for design bugs finds the potential fault candidates at RTL and gate-level of a circuit. Debug techniques for logic bugs and synchronization bugs are demonstrated, enabling readers to localize the most difficult bugs. Debug automation

for electrical faults (delay faults)finds the potentially failing speedpaths in a circuit at gate-level. The various debug approaches described achieve high diagnosis accuracy and reduce the debugging time, shortening the IC development cycle and increasing the productivity of designers. Describes a unified framework for debug automation used at both pre-silicon and post-silicon stages; Provides approaches for debug automation of a hardware system at different levels of abstraction, i.e., chip, gate-level, RTL and transaction level; Includes techniques for debug automation of design bugs and electrical faults, as well as an infrastructure to debug NoC-based multiprocessor SoCs.