

1. Record Nr.	UNINA990009536520403321
Autore	Immenga, Ulrich
Titolo	Die personalistische Kapitalgesellschaft = Eine rechtsvergleichende Untersuchung nach deutschem GmbH-recht und dem Recht der Corporations in der Vereinigten Staaten / Ulrich Immenga (a cura di)
Pubbl/distr/stampa	Germany : Athenaum Verlag GmbH, 1970
Descrizione fisica	443 p. ; 25 cm
Collana	Wirtschaftsrecht und Wirtschaftspolitik / Kurt Biedenkopf - Enrich Hoppman
Locazione	DEC
Collocazione	DPR 21-655 DPR 21*534
Lingua di pubblicazione	Tedesco
Formato	Materiale a stampa
Livello bibliografico	Monografia

2. Record Nr.	UNINA9910299847903321
Autore	Cerny Eduard
Titolo	SVA: The Power of Assertions in SystemVerilog / / by Eduard Cerny, Surrendra Dudani, John Havlicek, Dmitry Korchemny
Pubbl/distr/stampa	Cham : , : Springer International Publishing : , : Imprint : Springer, , 2015
ISBN	3-319-07139-4
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Descrizione fisica	1 online resource (589 p.)
Disciplina	004.1 621.381548
Soggetti	Electronic circuits Microprocessors Circuits and Systems Processor Architectures Electronic Circuits and Devices
Lingua di pubblicazione	Inglese
Formato	Materiale a stampa
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Note generali	Description based upon print version of record.
Nota di bibliografia	Includes bibliographical references and index.
Nota di contenuto	Part I. Opening -- Introduction -- System Verilog Language and Overview -- System Verilog Simulation Semantics -- Part II. Basic Assertions -- Assertion Statements -- Basic Properties -- Basic Sequences -- Assertion System Functions and Tasks -- Part III. Metalanguage Constructs -- Let, Sequence and Property Declarations; Inference.- Checkers -- Part IV. Advanced Assertions -- Advanced Properties -- Advanced Sequences.- Clocks -- Resets -- Procedural Concurrent Assertions.- An Apology for Local Variables -- Mechanics of Local Variables -- Recursive Properties -- Coverage -- Debugging Assertions and Efficiency Considerations -- Part V. Formal Verification -- Introduction to Assertion-Based Formal Verification.- Formal Verification and Models.- Formal Semantics.- Part VI. Advanced Checkers -- Checkers in Formal Verification.- Checker Libraries -- Appendix -- References.- Index.
Sommario/riassunto	This book is a comprehensive guide to assertion-based verification of hardware designs using SystemVerilog Assertions (SVA). It enables readers to minimize the cost of verification by using assertion-based

techniques in simulation testing, coverage collection, and formal analysis. The book provides detailed descriptions of all the language features of SVA, accompanied by step-by-step examples of how to employ them to construct powerful and reusable sets of properties. The book also shows how SVA fits into the broader SystemVerilog language, demonstrating the ways that assertions can interact with other SystemVerilog components. The reader new to hardware verification will benefit from general material describing the nature of design models and behaviors, how they are exercised, and the different roles that assertions play. This second edition covers the features introduced by the recent IEEE 1800-2012 SystemVerilog standard, explaining in detail the new and enhanced assertion constructs. The book makes SVA usable and accessible for hardware designers, verification engineers, formal verification specialists, and EDA tool developers. With numerous exercises, ranging in depth and difficulty, the book is also suitable as a text for students.

- Provides a comprehensive guide to assertion-based verification with SystemVerilog Assertions (SVA);
- Includes step-by-step examples of how SVA can be used to construct powerful and reusable sets of properties;
- Covers the entire SVA language with all the recent enhancements of the IEEE 1800-2012 SystemVerilog standard.
