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| Soggetti | Electronic circuits Power electronics Computer organization Circuits and Systems Power Electronics, Electrical Machines and Networks Computer Systems Organization and Communication Networks |
| Lingua di pubblicazione | Inglese |
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| Livello bibliografico | Monografia |
| Note generali | Description based upon print version of record. |
| Nota di bibliografia | Includes bibliographical references at the end of each chapters. |
| Nota di contenuto | Introduction -- Background -- Design and Simulation Results -- Top-Level Design -- Layout and Post-Layout Simulations -- Perspectives -- Transformer-Coupled Buffer. |
| Sommario/riassunto | This book describes the design of a receiver front-end circuit for operation in the 60GHz range in 90nm CMOS. Physical layout of the test circuit and post-layout simulations for the implementation of a test chip including the QVCO and the first stage divider are also presented. The content of this book is particularly of interest to those working on mm-wave frequency generation and signal reception. |