Record Nr. UNINA9910299830503321 Autore Saini Sandeep Titolo Low Power Interconnect Design [[electronic resource] /] / by Sandeep Saini New York, NY:,: Springer New York:,: Imprint: Springer,, 2015 Pubbl/distr/stampa **ISBN** 1-4614-1323-0 Edizione [1st ed. 2015.] Descrizione fisica 1 online resource (166 p.) 004.1 Disciplina 620 621.381 621.3815 Soggetti Electronic circuits **Electronics** Microelectronics Microprocessors Circuits and Systems Electronics and Microelectronics, Instrumentation **Processor Architectures** Inglese Lingua di pubblicazione **Formato** Materiale a stampa Livello bibliografico Monografia Note generali Description based upon print version of record. Nota di bibliografia Includes bibliographical references. Nota di contenuto Part I Basics of Interconnect Design -- Introduction to Interconnects --CMOS Buffer -- Part II Buffer and Schmidt trigger Insertion Techniques for Low Power Interconnect Design -- Buffer Insertion as a Solution to Interconnect Issues -- Schmidt Trigger Approach -- Part III Bus Coding Techniques for Low Power Interconnect Design -- Bus Coding Techniques. Sommario/riassunto This book provides practical solutions for delay and power reduction for on-chip interconnects and buses. It provides an in depth description of the problem of signal delay and extra power consumption, possible solutions for delay and glitch removal, while considering the power reduction of the total system. Coverage focuses

on use of the Schmitt Trigger as an alternative approach to buffer insertion for delay and power reduction in VLSI interconnects. In the

last section of the book, various bus coding techniques are discussed to minimize delay and power in address and data buses. · Provides practical solutions for delay and power Focuses on Deep reduction for on-chip interconnects and buses; · Sub micron technology devices and interconnects; . Offers in depth analysis of delay, including details regarding crosstalk and Describes use of the Schmitt Trigger as a versatile parasitics; · alternative approach to buffer insertion for delay and power reduction in VLSI interconnects; · Provides detailed simulation results to support the theoretical discussions. • Provides details of delay and power efficient bus coding techniques.