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Titolo	FPGA Design : Best Practices for Team-based Reuse // by Philip Andrew Simpson
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Descrizione fisica	1 online resource (260 p.)
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Soggetti	Electronic circuits Microprocessors Electronics Microelectronics Circuits and Systems Processor Architectures Electronics and Microelectronics, Instrumentation
Lingua di pubblicazione	Inglese
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Note generali	Description based upon print version of record.
Nota di contenuto	Introduction -- Project Management -- Design Specification -- System Modeling -- Resource Scoping -- Design Environment -- Board Design -- Power and Thermal analysis -- Team Based Design -- RTL Design -- IP reuse -- Embedded Design -- Functional verification -- Timing Closure -- High level Design -- In System Debug -- Design Sign-off.
Sommario/riassunto	This book describes best practices for successful FPGA design. It is the result of the author's meetings with hundreds of customers on the challenges facing each of their FPGA design teams. By gaining an understanding into their design environments, processes, what works and what does not work, key areas of concern in implementing system designs have been identified and a recommended design methodology to overcome these challenges has been developed. This book's content has a strong focus on design teams that are spread across sites. The

goal being to increase the productivity of FPGA design teams by establishing a common methodology across design teams; enabling the exchange of design blocks across teams. Coverage includes the complete FPGA design flow, from the basics to advanced techniques. This new edition has been enhanced to include new sections on System modeling, embedded design and high level design. The original sections on Design Environment, RTL design and timing closure have all been expanded to include more up to date techniques as well as providing more extensive scripts and RTL code that can be reused by readers. Presents complete, field-tested methodology for FPGA design, focused on reuse across design teams; Offers best practices for FPGA timing closure, in-system debug, and board design; Details techniques to resolve common pitfalls in designing with FPGAs.
