1. Record Nr.             UNINA9910299760503321

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   Titolo                Designing 2D and 3D network-on-chip architectures / / Konstantinos Tatas [and three others]

   Pubbl/distr/stampa    New York : , : Springer, , 2014

   ISBN                  1-4614-4274-5

   Edizione              [1st ed. 2014.]

   Descrizione fisica    1 online resource (xiii, 265 pages) : illustrations (some color)

   Collana               Gale eBooks

   Disciplina            621.392

   Soggetti              Networks on a chip - Design and construction

   Lingua di pubblicazione   Inglese

   Formato               Materiale a stampa

   Livello bibliografico Monografia

   Note generali         Description based upon print version of record.

   Nota di bibliografia  Includes bibliographical references.

   Nota di contenuto     Part I: Network-on-Chip Design Methodology -- Network-on-Chip Technology: A Paradigm Shift -- NoC Modeling and Topology Exploration -- Communication Architecture -- Power and Thermal Effects and Management -- NoC-based System Integration -- NoC Verification and Testing -- The Spidergon STNoC -- Middleware Memory Management in NoC -- On Designing 3-D Platforms -- The SYSMANTIC NoC Design and Prototyping Framework -- Part II: Suggested Projects.-  Projects on Network-on Chip.

   Sommario/riassunto    This book covers key concepts in the design of 2D and 3D Network-on-Chip interconnect.  It highlights design challenges and discusses fundamentals of NoC technology, including architectures, algorithms and tools.  Coverage focuses on topology exploration for both 2D and 3D NoCs, routing algorithms, NoC router design, NoC-based system integration, verification and testing, and NoC reliabilty.  Case studies are used to illuminate new design methodologies. ·         Describes essential theory, practice and state-of-the-art applications of 2D and 3D Network-on-Chip interconnect; ·         Enables readers to exploit parallelism in processor architecture, with interconnect design that is efficient in terms of energy and performance; ·         Covers topics not available in other books, such as NoC and distributed memory organization, dynamic memory management and abstract data type support in many-core platforms, and distributed hierarchical power management.