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Titolo	System Verilog assertions and functional coverage : guide to language, methodology and applications // Ashok B. Mehta
Pubbl/distr/stampa	New York, : Springer, c2014
ISBN	1-4614-7324-1
Descrizione fisica	1 online resource (xxxiii, 356 pages) : illustrations (some color)
Collana	Gale eBooks
Disciplina	004.1 620 621.381 621.3815
Soggetti	Computer hardware description languages Verilog (Computer hardware description language)
Lingua di pubblicazione	Inglese
Formato	Materiale a stampa
Livello bibliografico	Monografia
Note generali	Includes index.
Nota di contenuto	Introduction -- System Verilog Assertions -- Immediate Assertions -- Concurrent Assertions -- Basics (sequence, property, assert).- Sampled Value Functions \$rose, \$fell -- Operators -- System Functions and Tasks -- Multiple clocks -- Local Variables -- Recursive property -- Detecting and using endpoint of a sequence -- 'expect' -- 'assume' and formal (static functional) verification -- Other important topics -- Asynchronous Assertions !!! -- IEEE-1800--2009 Features -- SystemVerilog Assertions LABs -- System Verilog Assertions -- LAB Answers -- Functional Coverage -- Performance Implications of coverage methodology -- Coverage Options (Reference material).
Sommario/riassunto	This book provides a hands-on, application-oriented guide to the language and methodology of both System Verilog Assertions and System Verilog Functional Coverage. Readers will benefit from the step-by-step approach to functional hardware verification, which will enable them to uncover hidden and hard to find bugs, point directly to the source of the bug, provide for a clean and easy way to model complex timing checks and objectively answer the question 'have we functionally verified everything'. Written by a professional end-user of both System Verilog Assertions and System Verilog Functional

Coverage, this book explains each concept with easy to understand examples, simulation logs and applications derived from real projects. Readers will be empowered to tackle the modeling of complex checkers for functional verification, thereby reducing drastically their time to design and debug. Covers both System Verilog Assertions and System Verilog Functional Coverage language and methodologies; Provides practical examples of the what, how and why of Assertion Based Verification and Functional Coverage methodologies; Explains each concept in an easy to understand, step-by-step fashion and applies it to a real example; Includes practical labs that enable readers to put in practice the concepts explained in the book.
