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| Autore                  | Paul Somnath   |
| Titolo                  | Computing with memory for energy-efficient robust systems // Somnath Paul, Swarup Bhunia   |
| Pubbl/distr/stampa      | New York : , : Springer, , 2014  |
| ISBN                    | 1-4614-7798-0  |
| Edizione                | [1st ed. 2014.]  |
| Descrizione fisica      | 1 online resource (xiii, 210 pages) : illustrations (some color)   |
| Collana                 | Gale eBooks  |
| Disciplina              | 004.1<br>620<br>621.381<br>621.3815  |
| Soggetti                | Nanoelectromechanical systems<br>Computer engineering  |
| Lingua di pubblicazione | Inglese  |
| Formato                 | Materiale a stampa   |
| Livello bibliografico   | Monografia   |
| Note generali           | Description based upon print version of record.  |
| Nota di bibliografia    | Includes bibliographical references.   |
| Nota di contenuto       | Part I Introduction -- Challenges in Computing for Nanoscale Technologies -- A Survey of Computing Architectures -- Motivation for a Memory-Based Computing Hardware -- Part II Memory Based Computing -- Key Features of Memory-Based Computing -- Overview of Hardware and Software Architectures -- Application of Memory-Based Computing -- Part III Hardware Framework -- A Memory Based Generic Reconfigurable Framework -- MAHA Hardware Architecture -- Part IV Software Framework -- Application Analysis -- Application Mapping to MBC Hardware.   |
| Sommario/riassunto      | This book analyzes energy and reliability as major challenges faced by designers of computing frameworks in the nanometer technology regime. The authors describe the existing solutions to address these challenges and then reveal a new reconfigurable computing platform, which leverages high-density nanoscale memory for both data storage and computation to maximize the energy-efficiency and reliability. The energy and reliability benefits of this new paradigm are illustrated and the design challenges are discussed. Various hardware and software aspects of this exciting computing paradigm are described, particularly with respect to hardware-software co-designed frameworks, where the |

hardware unit can be reconfigured to mimic diverse application behavior. Finally, the energy-efficiency of the paradigm described is compared with other, well-known reconfigurable computing platforms.

- Introduces new paradigm for hardware reconfigurable frameworks, which leverages dense memory array as a malleable resource, which can be used for information storage as well as computation;
- Merges spatial and temporal computing to minimize interconnect overhead and achieve better scalability compared to state-of-the-art reconfigurable computing platforms;
- Enables efficient mapping of diverse data-intensive applications from domains of signal processing, multimedia and security applications.

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